# 23. Packaging of Electronic Equipments (2)

## 23.1 Packaging and Interconnection Techniques

### Introduction

Electronic packaging, which for many years was only an afterthought in the design and manufacture of electronic systems, increasingly is being recognized as the critical factor in both cost and performance.

Current electronic systems employ a packaging technology which limits system performance because of a number of factors. As the circuit density on a chip goes up, the speed of functions it performs increases, Retention of signal integrity is another consideration, the power needed to run the chips generates significant amounts of heat which must necessarily be removed an important requirement. The selection of packaging and interconnection techniques is a very complex task for the designer and manufacturing engineer where the selection depends on a number of driving forces: mechanical, electrical, and thermal force.

### 23.1.1 Mechanical requirements

The mechanical diving force strives to attain technology advancements to keep pace with the considerable improvements being made by the continued reduction (per function) in the integrated circuit package size.

### 23.1.2 Electrical requirements

The electrical driving force is bringing new technology to the fabricator of conventional PWBs, with expressions such as controlled impedance, dielectric constant, insulation resistance. Improvements in dimensional stability and registration accuracy and use of new (more expensive) materials are the result of attempting to satisfy these needs.

### 23.1.3 Thermal requirements

Thermal driving forces are threefold. In one case, it is giving credence to the use of materials and processes that can satisfy the higher assembly processing temperatures to which the PWBs must be subjected, that is, materials with a higher glass transition temperature (Tg). Another instance concerns coefficient of thermal expansion which has resulted in some applications using reinforced metal planes or constraining metal cores. In third instance, the printed board becomes an active element in the thermal management of the assemblies cooling systems.

The different advanced packaging and interconnection techniques as shown in the Figure 23.1.

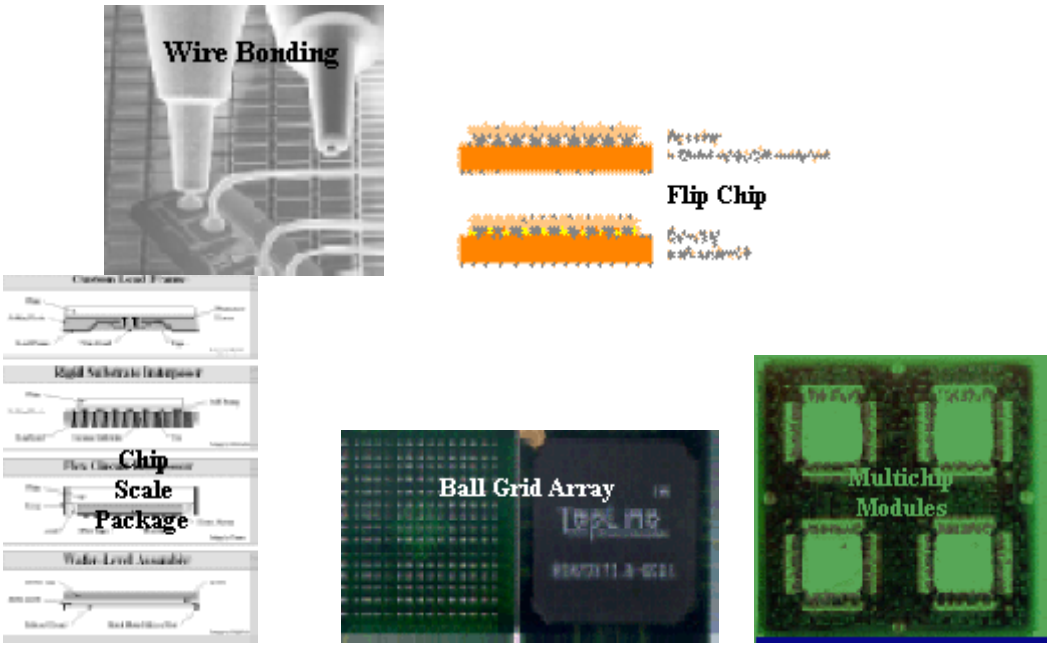


Figure23.1 Different packaging and interconnection techniques used in manufacturing

## 23.2 Electronics Packaging Levels

There are six generally recognized levels of electronic packaging. Figure 23.2 shows the general packaging levels. The six levels are:

- **Level 0:** Bare semiconductor (unpackaged).
- **Level 1:** Packaged semiconductor or packaged electronic functional device. There are two cases to be distinguished regarding packaged IC devices. The first case entails a single semiconductor microcircuit within a suitable package.. The second case entails several semiconductor microcircuits plus discrete chips on a suitable substrate. This entire package is generally referred to as a multichip module (MCM).
- **Level 2:** Printed wiring assembly (PWA).This level involves joining the packaged electronic devices to a suitable substrate material. The substrate is most often an organic material such as FR-4 epoxy-fiberglass board, or ceramic such as alumina. Level 2 is sometimes referred to as the circuit card assembly (CCA) or, more simply, the card assembly.
- **Level 3:** Electronic subassembly. This level refers to several printed wiring assemblies (PWAs), normally two, bonded to a suitable backing functioning both as a mechanical support frame and a thermal heat sink. Sometimes this backing, or support frame, is called a subchassis. In some packaging hierarchies, e.g., computer packaging, Level 3 is the electronic assembly, also called the electronic box. As shown in Figure23.3.
- **Level 4:** Electronic assembly. This level consists of a number of electronic subassemblies mounted in a suitable frame. An electronic assembly, then, is a mechanically and thermally complete system of electronic subassemblies. This level is sometimes referred to as the electronic box or simply box level.
- **Level 5:** System. This refers to the completed product.

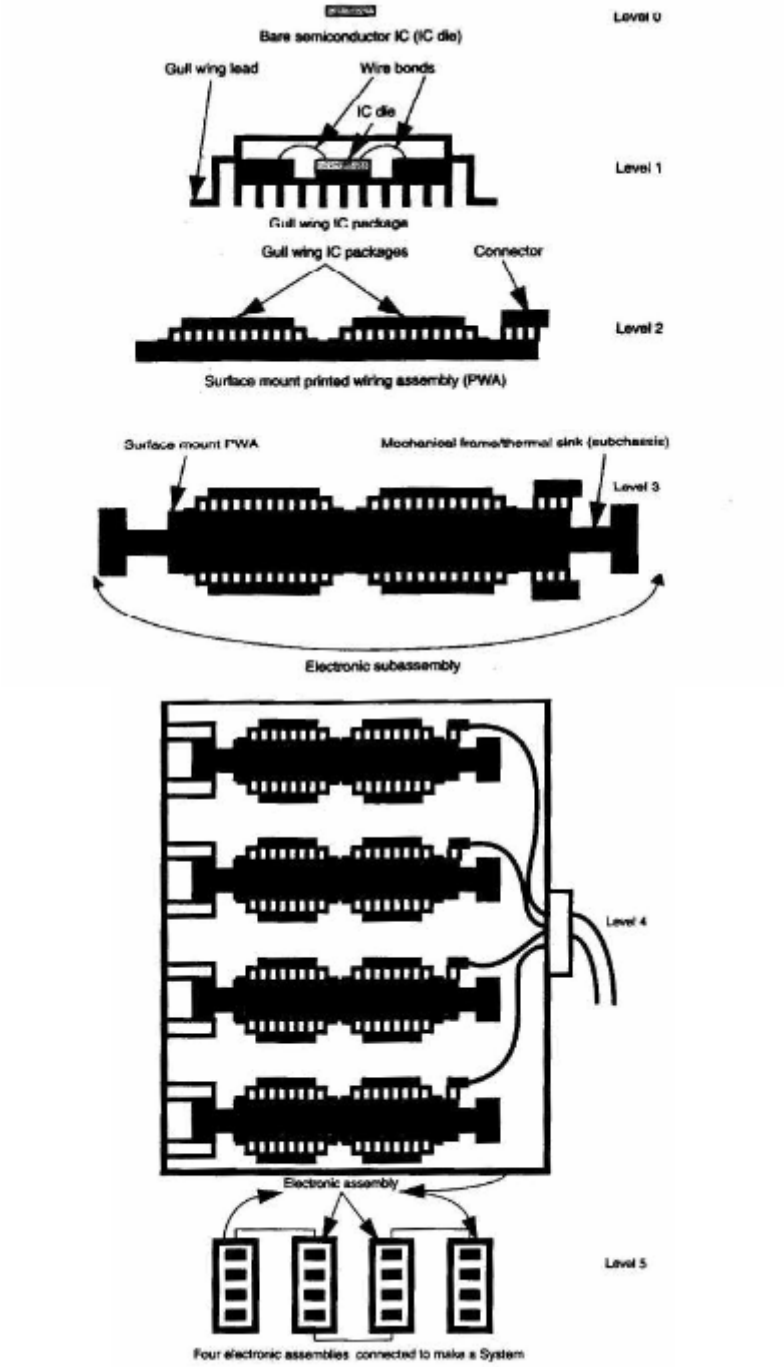


Figure 23.2 Packaging levels

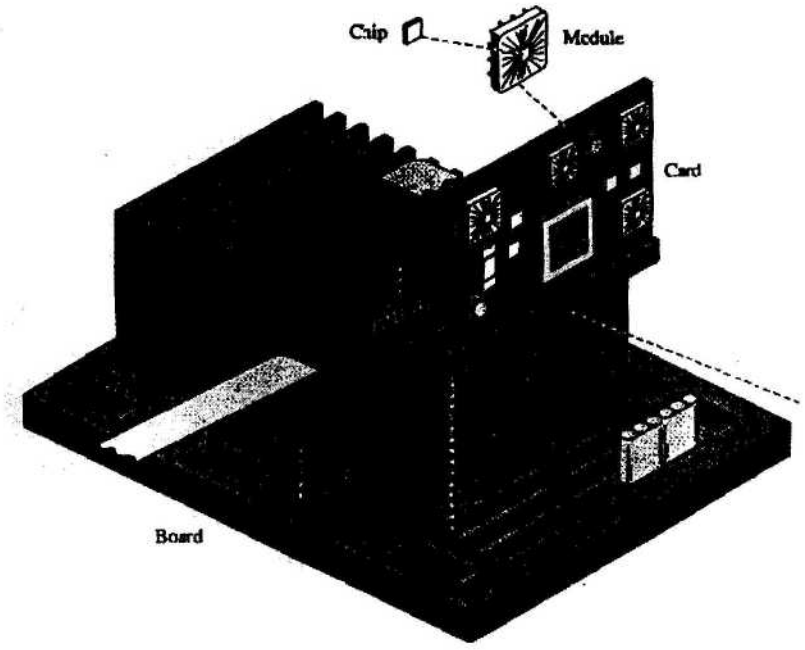


Figure23.3 Level 3 packaging

## 23.3 Wire Bonding Packaging

Wire bonding packaging also called chip-on-board packaging is the earliest technique of device assembly, whose first result was published by Bell Laboratories in 1957. Sine then, the technique has been extremely developed. Wire bonding, as the dominant chip-connection technology, has been used with all styles of microelectronic packages, from small individual chip packages to large, high-density multichip modules.
Virtually all dynamic random access memory (DRAM) chips and most commodity chips in plastic packages are assembled by wire bonding. About 1.2-1.4 trillion wire interconnections are produced annually.

In wire bonding (chip-and-wire) packaging, the IC chip is bonded directly on an interconnecting substrate either a printed wiring board or hybrid-and protected with a top encapsulant against moisture as shown in Figure23.4.

The encapsulants are materials such as silicone or epoxy which does provide very good moisture sealing in applications where high reliability is required.

Wire bonding is an electrical interconnection technique using thin wire and a combination of heat, pressure and/or ultrasonic energy. Wire bonding is a solid phase welding process, where the two metallic materials (wire and pad surface) are brought into intimate contact. Once the surfaces are in intimate contact, electron sharing or interdiffusion of atoms takes place.

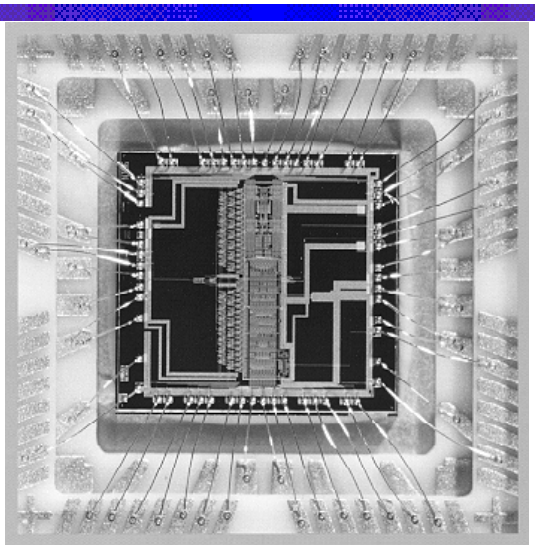

Figure 23.4 Chip interconnection using wire bonding technology

### 23.3.1 Wire Bonding Process

There are three types of wire bonding processes: thermocompression, ultrasonic, and thermosonic bonding.

**Thermocompression wire bonding:**

Thermocompression wire bonding is the most frequently used in wire bonding process .The principle is to join two metals using heat and pressure but without melting. The elevated temperature maintains the metals in annealing state as they join in molecular metallurgical bond (e.g. heating up to 300 $^{o}$C for gold bonding). In order to avoid pre-damaging the material, the bonding force must be applied with a gradient, the process of bonding as shown in Figure 23.5.

**Ultrasonic wire bonding:**

Ultrasonic bonding is a different concept of bonding that uses pressure in addition to rapid scrubbing or wiping to achieve a molecular bond. The scrubbing action effectively removes any oxide films that may be present. Extreme care must be taken so that the chip is not damaged during the ultrasonic wire-bonding action. Since ultrasonic energy softens the bonding material and makes it easy to plastic deformation, ultrasonic bonding can create bonds between wide varieties of materials.

**Thermosonic wire bonding:**

Ultrasonic energy is used with thermocompression wire bonding methods, resulting in a technique known as Thermosonic wire bonding**.** The process depends on vibrations created by ultrasonic action to scrub the bond area to remove any oxide layers and create the heat necessary for wire bonding.

The main benefit of the method compared to thermocompression is lower bonding temperature and shorter processing time.

The comparison between the three bonding processes as shown in Table 23.1.

Table 23.1 Three wire bonding processes

| Wire bonding | Pressure | Temperature | Ultrasonic energy |
|---|---|---|---|
| Thermocompression | High | 300-500 $^{o}$C | No |
| Ultrasonic | Low | 25 $^{o}$C | Yes |
| Thermosonic | Low | 100-150 $^{o}$C | Yes |

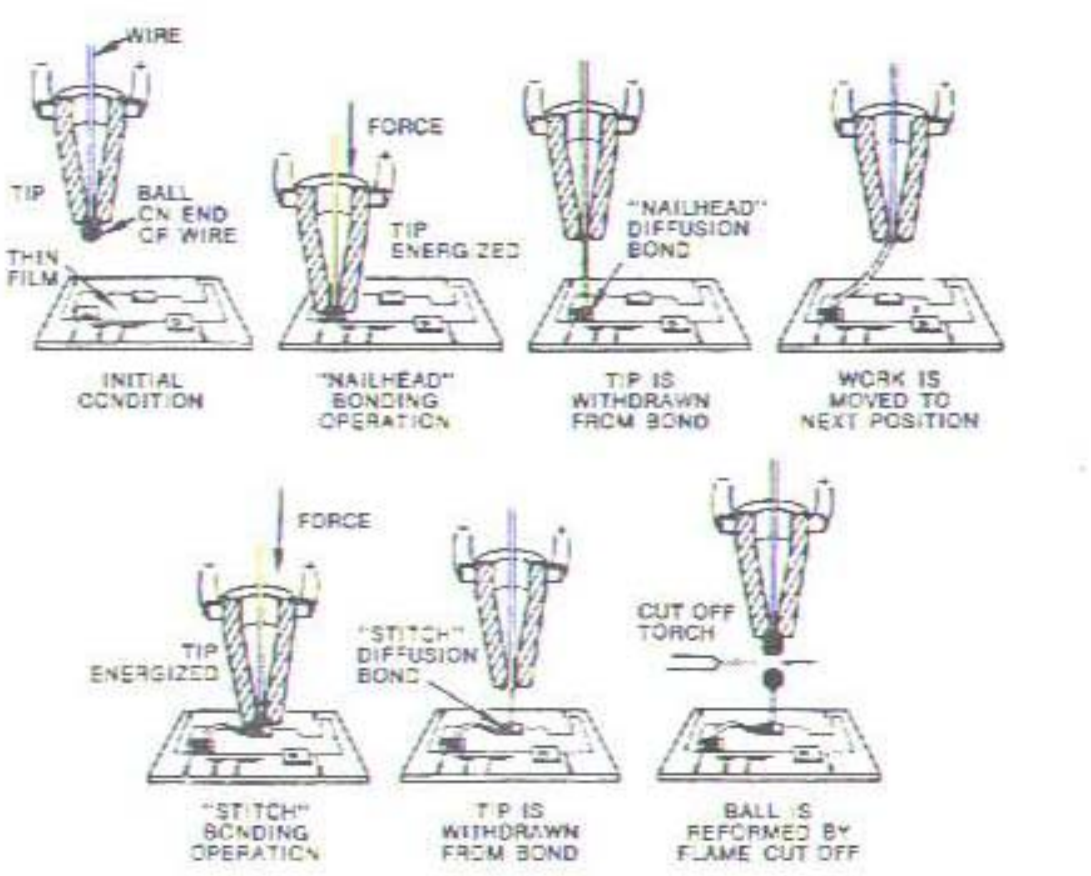


Figure 23.5 Wire bonding steps with thermocompression bonding

## 23.3.2 Wire Bonding Techniques

The basic method actually includes two different bonding techniques: wedge, and ball bonding.

Approximately 93% of all semiconductor packages are manufactured using ball bonding method, while wedge bonding is used to produce about 5% of all assembled packages.

### 23.3.2.1 Ball Bonding

In this technique, wire is passed through a hollow capillary, and an electronic-flame-off system (EFO) is used to melt a small portion of the wire extending beneath the capillary. The surface tension of the molten metal forms a spherical shape or ball. The ball is pressed to the bonding pad on the die with sufficient force to cause plastic deformation and atomic interdiffusion of the wire and the underlying metallization, which ensure the intimate contact between the two metal surfaces and form the first bond (ball bond). The capillary is then raised and repositioned over the second bond site on the substrate as shown in Figure 23.6; a

precisely shaped wire connection called a wire loop is thus created as the wire goes. Deforming the wire against the bonding pad makes the second bond (wedge bond or stitch bond), having a crescent shape (as shown in Figure23.7) made by the imprint of the capillary's outer geometry. Then the wire clamp is closed, and the capillary ascends once again, breaking the wire just above the wedge, an exact wire length is left for EFO to form a new ball to begin bonding the next wire. This technique requires a high temperature raging from 100$^{o}$C to 500$^{o}$C depending on bonding process. Heat is generated during the manufacturing process either by a heated capillary feeding the wire or by a heated pedestal on which the assembly is placed or by both depending on the bonding purpose and materials.

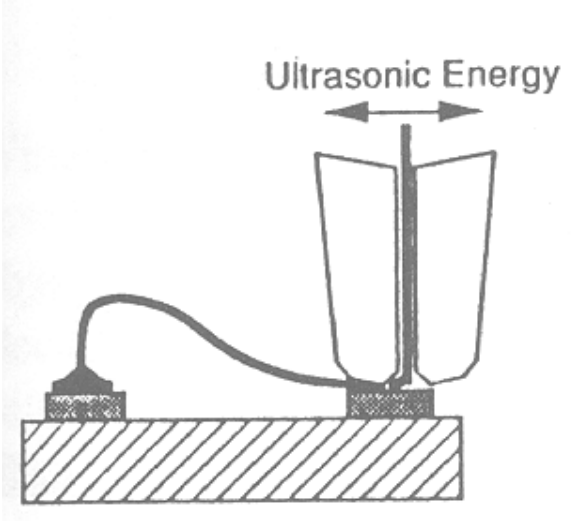


Figure 23.6 Ball bonding technique

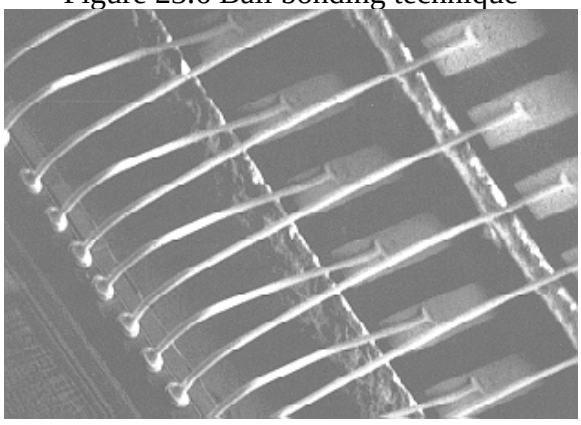

Figure 23.7 Application of ball bonding

**23.3.2.2 Wedge Bonding**

Wedge bonding is named based on the shape of its bonding tool. In this technique, the wire is fed at an angle usually 30-60$^{o}$ from the horizontal bonding surface through a hole in the back of a bonding wedge. By descending the wedge onto the IC bond pad, the wire is pinned against the pad surface and an Ultrasonic or thermosonic is performed. Next, the wedge rises and executes a motion to create a desired loop shape. At the second bond location, the wedge descends, making a second bond.

Wedge bonding technique can be used for both aluminum wire and gold wire bonding applications. The principle difference between the two processes is that the aluminum wire is bonded in an ultrasonic bonding process at room temperature as shown in Figure 23.8,

whereas gold wire wedge bonding is performed through a thermosonic bonding process with heating up to 150 $^{o}$C. A considerable advantage of the wedge bonding is that it can be designed and manufactured to very small dimensions. Aluminum ultrasonic bonding is the most common wedge bonding process because of the low cost and the low working temperature. The main advantage for gold wire wedge bonding is the possibility to avoid the need of hermetic packaging after bonding due to the inert properties of the gold. In addition, a wedge bond will give a smaller footprint than a ball bond as shown in Figure 23.9, which specially benefits the microwave devices with small pads that require a gold wire junction.

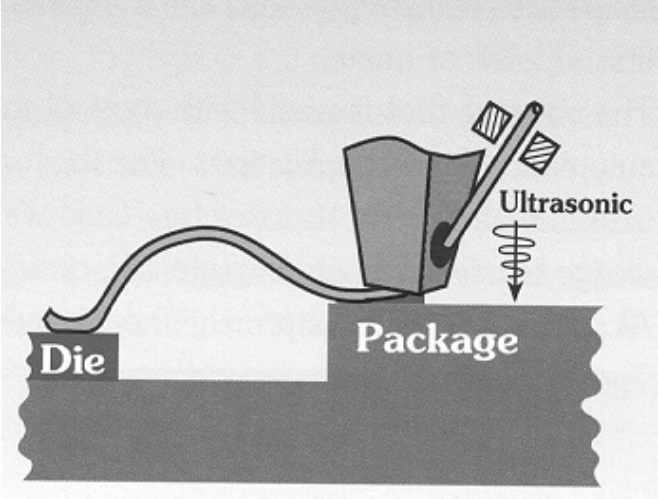


Figure 23.8 Ultrasonic wedge bonding

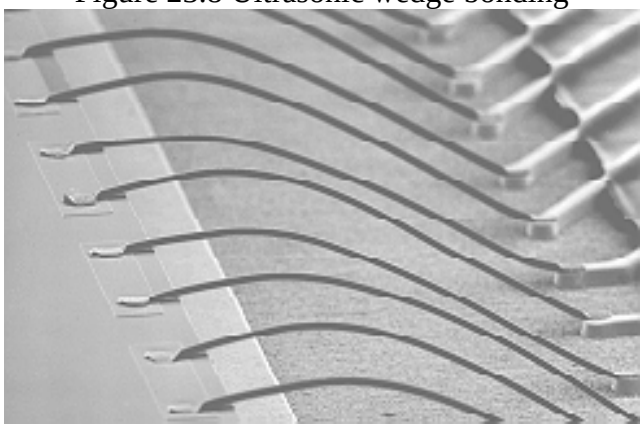

Figure 23.9 Application of wedge bonding

### 23.3.3 Cost

The main cost of wire bonding method includes:

- Wire bonder
- Die attach equipment.
- Support equipment
- Materials including tool, wire, die attach materials.
- Engineering.

Cost analysis should include volume and individual process cycle time predictions.

## 23.4 Flip-Chip Packaging

In the development of packaging of electronics the aim is to lower cost, increase the packaging density, and improve the performance while still maintaining or even improving the reliability of the circuits. The concept of flip-chip process where the semiconductor chip is assembled directly face down onto circuit board.

Flip-chip joining is not a new technology. The technology has been driven by IBM for mainframe computer applications. Many millions of flip-chips have been processed by IBM on ceramic substrates since the end of 60`s. At the beginning of 70`s the automotive industry also began to use flip-chips on ceramics. Today flip-chips are widely used for watches, mobile phones, portable communicators, disk drives, hearing aids, LCD displays, automotive engine controllers as well as the main frame computers. The number of flip-chips assembled was over 500 million in year 1995 and close to 600 million flip chips were consumed 1997.

### 23.4.1 Flip-Chip Process by Solder Joining

The flip-chip concept process employed small, solder-coated copper balls (electrically conducting bumps) sandwiched between the chip and the substrate, and may the flip-chip joints without or with underfill material are shown in Figure23.10.

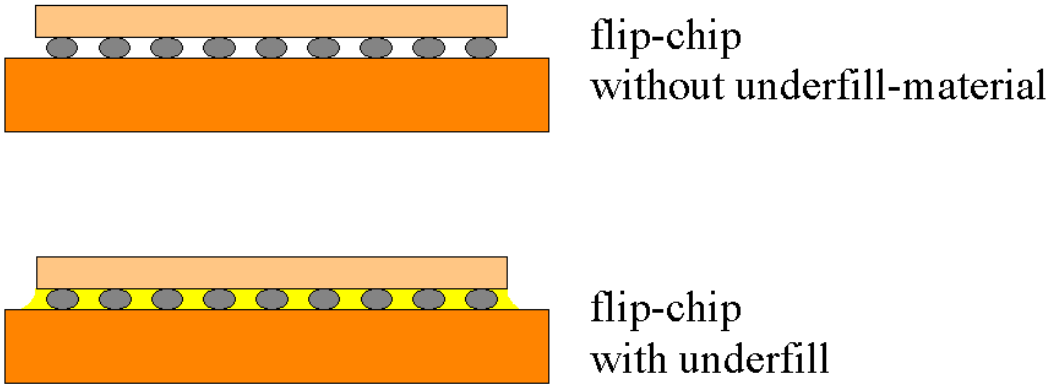


Figure 23.10.Cross sections of flip-chip joints without and with underfill material.

Tacky flux is applied to the solder contact areas by dipping the chip into a flux reservoir or by dispensing flux onto the substrate. The bumps of chips are placed into the tacky paste and they are reflowed in an oven to drive off any flux residues. After the reflow process cleaning of the flux is preferred. If the solder reflow has been accomplished correctly the flip-chip solder joints will be smooth, and shiny. The underfill material is applied by dispensing along one or two sides of the chip, from where the low viscosity epoxy is drawn by capillary forces into the space between the chip and substrate as shown in Figure23.11. Finally the underfill is cured by heat. Repairing of the flip-chip joint is usually impossible after the underfill process. Therefore testing must be done after reflow and before the underfill application.

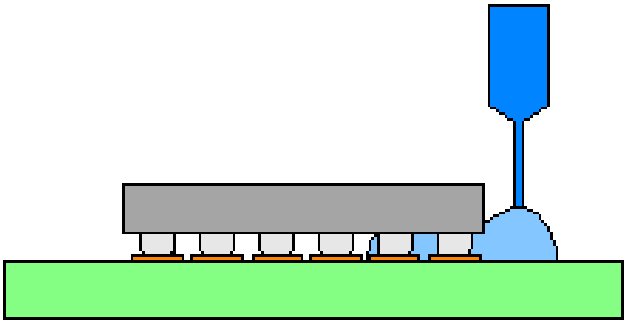

Figure 23.11.the underfill application by dispensing.

### 23.4.2 Flip-Chip Joining

The flip-chip joining mainly by thermocompression or thermosonic processes as shown in Figure 23.12. In the thermocompression bonding process, the bumps of the chip are bonded to the pads on the substrate by force and heat applied from an end effector. The bonding temperature is usually high, e.g. 300 $^{o}$C for gold bonding, to soften the material and increase the diffusion bonding process. The bonding force can be up to 1 N for an 80μm diameter bump. Due to the required high bonding force and temperature, the process is limited to rigid substrates such as alumina or silicon. A bonder with high accuracy in the parallelism alignment is required. In order to avoid pre-damaging of the semiconductor material, the bonding force must be applied with a gradient.

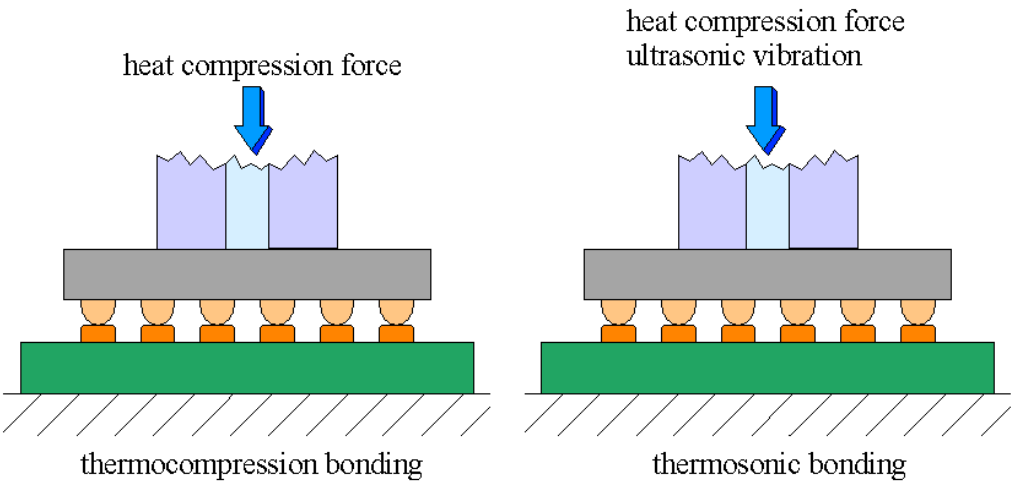


Figure 23.12 Principles of flip-chip joining by thermocompression and thermosonic processes

The thermocompression bonding process can be made more efficient by using ultrasonic power to speed up the welding process. Ultrasonic energy is transferred to the bonding area from the pick-up tool through the back surface of the chip. The thermosonic bonding introduces ultrasonic energy that softens the bonding material and makes it easy to plastic deformation.

### 23.4.3 General Advantages and Disadvantages using Flip-Chip Technology

**Advantages:**

- Improved thermal capabilities: Because flip-chips are not encapsulated, the back side of the chip can be used for efficient cooling.
- The chip is capable of handling a high number of I /Os because solder bumps can be arranged in an area array rather than being restricted to the chip's periphery.
- Due to surface tension factors related to the solder, this technique has a self-aligning during bonding.
- Improved performance due to short interconnect distance: delivers low inductance, resistance and capacitance, and small electrical delays.

**Disadvantages:**

- Difficult testing the joints. For inspection of hidden joints X-ray equipment is needed.
- Flux removal is difficult.
- High assembly accuracy needed.
- Low reliability for some substrates.
- Repairing is difficult or impossible.

### 23.4.4 Relative Cost Comparison

Cost of flip-chip process is less than half of the corresponding cost for wire bonding technology and the floor space needed is also only about one half of that for wire bonding technology.

The cost of flip-chip technology can be divided into bumping cost and assembly process cost. The assembly processes for the most common flip-chip technology include pick and place together with flux application, reflow and cleaning as well as underfill process. The cost of the necessary equipment and floor space, the capacity of the equipment and its compatibility with other manufacturing processes are also important factors having influence on the economy of the technology for particular product. The substrate has also an important impact on the packaging costs. The cost of substrate depends e.g. on via sizes, layer count, line width and spaces, die pad pitch, flatness requirements, material type and the fabrication process.

## 23.5 Chip Scale Packaging

Chip Scale Packaging combines the best of flip chip assembly and surface mount technology. The Chip Scale Packaging Task Force carried out between 1996 and 1997 and a project work carried out by two students at Chalmers University of Technology.

### 23.5.1 Description of Various Types of CSPs

CSPs are often classified based on their structure. At least four major categories have been proposed. These are: Flex circuit interposer, rigid substrate interposer, custom lead frame, and wafer-level assembly. Examples of packages of these categories are given in Figure 23.13.

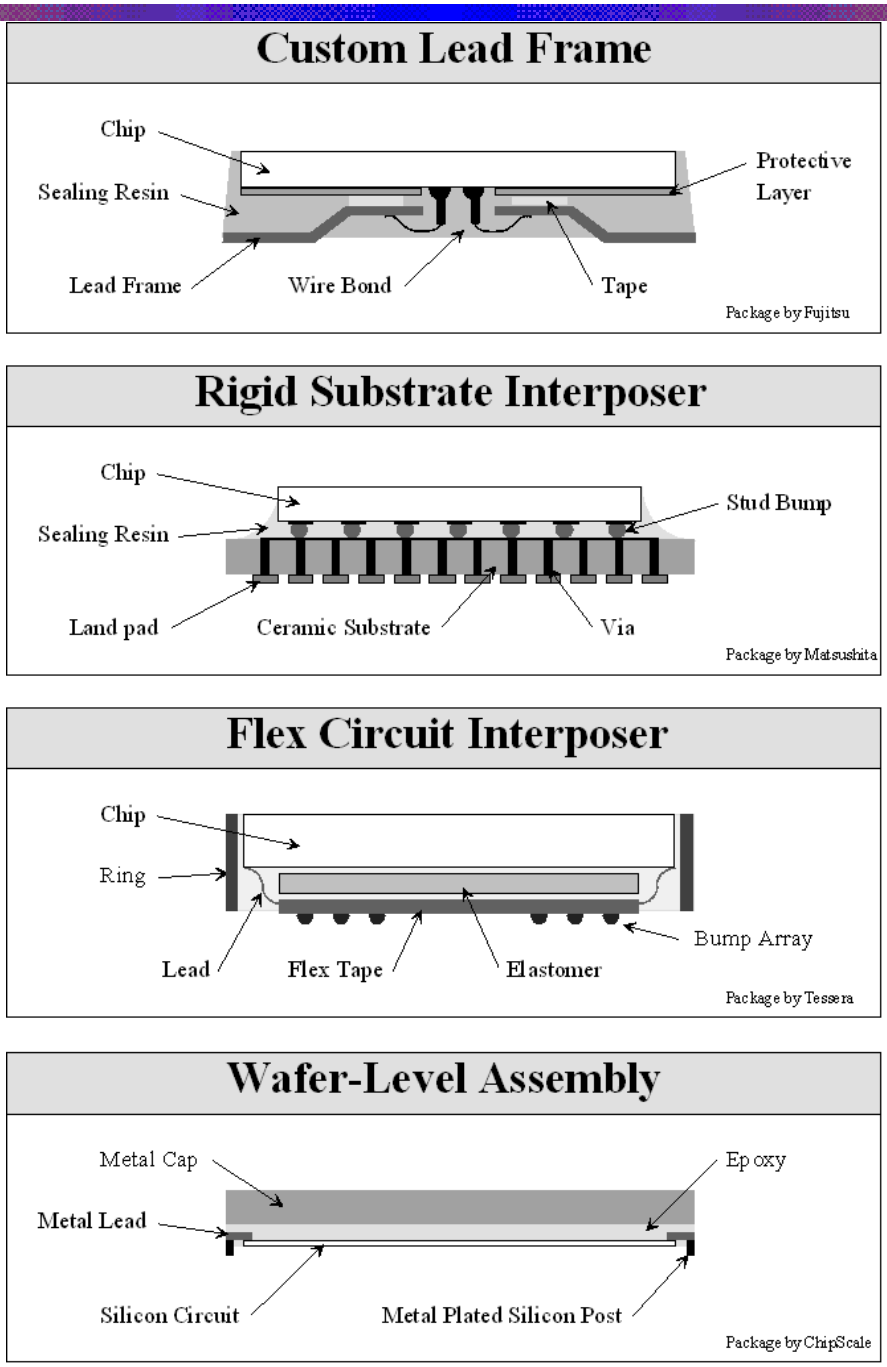


Figure23.13 Main CSP categories

The main driving forces for using CSPs are:

- Improvement in performance
- Size and weight reduction
- Easier assembly process

Of these, reduction of size and weight are probably the most important factors for selection of CSP technology. Consequently, consumer products like camcorders, mobile phones, and laptops gare among the products that have been first to utilise CSPs.

## 23.5.2 Production Issues

### 23.5.2.1 Assembly Issues

Most CSPs can be mounted using current fine pitch SMT assembly materials and processes. Vision systems may have problem recognising the structure of some CSPs. In addition, some packages are moisture sensitive. That is, they must be stored in dry conditions and used within a specified time frame after they have been exposed to humid environments. If the time frame is surpassed, or if a package needs to be reworked, it should be baked before any work is performed.

### 23.5.2.2 Tools and Investments

As pitches for CSP may get smaller conventional pick & placement machines may not suffer for mounting of the components which then will necessitate investments in new advanced machines. Also, X-ray equipment may be necessary for inspection for verification of solder joints. In cases when underfills must be used of reliability reasons, material and equipment for the underfilling process will add to the total cost.

## 23.5.3 Price

Only a few CSPs are in production today and then in low volume production. Therefore, it is difficult to get information of what the price will be for various CSPs. Furthermore, the large variations in construction of the various package types will also affect the production costs for the various packages. Many company forecast that the cost initially will be 10 to 50 % higher than conventional packages and that cost equality will be reached when they are produced in high volumes.

# 23.6Ball Grid Array Packaging

The information presented in this technique has been collected from a number of sources describing BGA activities, the most important of the former being the Swedish National Research Programme "BGA Modules for Automotive Electronics in Harsh Environments", and carried out between 1994 and 1997.

The Quad Flat Pack (QFP) and the Ball Grid Array (BGA) packages today both offer a large number of I/Os, as required by modern IC technology. The peripheral QFP technology is fragile leads around the periphery-all four sides. The BGA taking advantage of the area under the package for the solder sphere interconnections in an array to increase both the numbers of I/Os and pitch.

Figure 23.14 below illustrates the difference between QFP and BGA packages, showing an ultra fine-pitch 160 lead QFP (pitch 0.3 mm) on a background consisting of the bottom side of a 1.5 mm pitch PBGA with 225 interconnection solder balls. From this picture it is easy to understand the popularity this BGA package has received among the people in the assembly business. Note that there are five QFP leads for every BGA solder sphere period.


Figure 23.14 A 160-lead 0.3 mm pitch QFP placed on a grid of 1.5 mm pitch spheres (bottom side of a PBGAS225)

A BGA package can typically be characterized by the following general statements:

- It is an IC package for active devices intended for surface mount applications.
- It is an area array package, i.e. utilizing whole or part of the device footprint for interconnections.
- The interconnections are made of balls (spheres) of most often a solder alloy or sometimes other metals. The length of the package body (most often square) ranges from 7 to 50 mm.
- The pitch, i.e. center-to-center distance, of the balls is generally between 1.0 and 1.5 mm.

### 23.6.1 Types of BGA Packages

The PBGA is one of the most types in BGA and another types of BGA packages such as the TBGA (Tape BGA), presented. Also outside the scope of this text is the multichip moudule - or MCM-BGAs, which are similar in construction to ordinary BGAs, but contain two or more chips inside the package.

### 23.6.1.1 PBGA (Plastic Ball Grid Array)

In plastic ball grid array (PBGA), a die is mounted to the top side of substrate, double-sided PWB as shown in Figure 23.15.

The silicon chip containing the integrated circuit is die bonded to the top surface of the substrate.

The over-molded or glop-top encapsulation is then preformed to completely cover the chip, wires and substrate bond pads. Interconnection of signal and power lines between the die and the PW-board contact points is through thermosonic gold wire bonding. From there, copper traces are routed to an array of metal pads on the bottom of the printed wiring board. . Most often a two sided substrate metallization is sufficient to provide electrical contacts from wire-bonds through plated through-holes are usually around the periphery of the board to solder ball pads. The substrate is generally is made of 0.25 mm thick BT (bismaleimide-triazine) epoxy glass laminate with 18 µm copper thickness. In addition, thermal balls under the center of the package are often used to remove heat from the device through thermal vias.

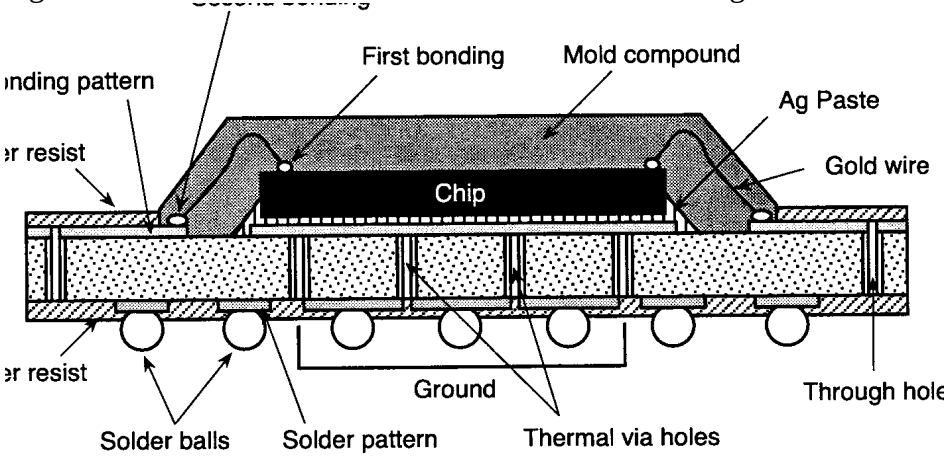


Figure 23.15.Across-section of a typical PBGA

### 23.6.1.1 TBGA (Tape or Tab Ball Grid Array)

Another interesting, but not yet so common type of BGA package, is the Tape or Tab BGA gets their name from the tape (a flexible polyimide conductor film with copper metallization) automated bonding (Tab) type frame that connects the chip with the next level board (Card).

Solder attachment balls of high temperature 10Sn90Pb alloy are used with diameter is usually 0.63 mm for a package pitch of 1.27 mm. The back of the chip can be put in direct contact with a thermally conductive adhesive to provide efficient transport of heat to the metal cover or heat sink to easily dissipate 10 to 15 W, as shown in Figure 23.16.

Current TBGA packages ranges from 21 to 40mm body size with 192 to 736 I/O connections.

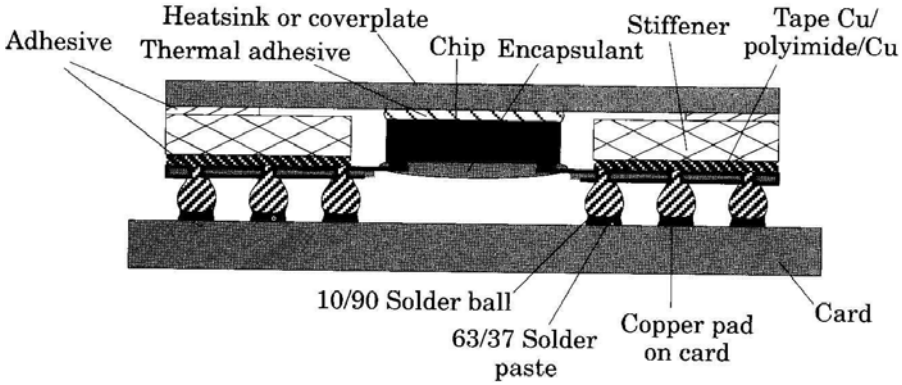


Figure 23.16 Cross-section of a Tape (or TAB) BGA – TBGA

## 23.5.2 Advantages and Disadvantages using BGAs

**Advantages:**

- BGAs are less fragile and easier to handle both before and during assembly.
- A much higher assembly yield is generally expected using BGAs.
- The smaller package size with higher I/O devices.
- Reduced manufacturing cycle time.
- The package can be hermetically sealed.

**Disadvantages:**

- Cost is high.
- Inspection of the solder joints is impossible without costly x-ray equipment.
- Board level rework potentially more difficult.