22. Packaging of Electronic Equipments (1)

22.1Printed Wiring Boards (PWBs)

Introduction

Printed-wiring boards, commonly called PWBs, are sometimes referred to as the baseline in electronic packaging. Electronic packaging is fundamentally an interconnection technology and the PWB is the baseline building block of this technology. It serves a wide variety of functions. Foremost, it contains the wiring required to interconnect the component electrically and acts as the primary structure to support those components. In some instances it is also used to conduct away heat generated by the components.

22.2 Printed Wiring Board Types

PWBs can be classified into several categories based on their dielectric material or their fabrication technique. This section describes PWBs fabricated using organic dielectric, ceramic dielectric, and discrete wire techniques.

22.2.1 Organic PWBs

These PWBs are fabricated using an organic dielectric material with copper usually forming the conductive paths. The organic-based boards can be subdivided into the following classifications: rigid, flexible, rigid-flex combining the attributes of both rigid and flexible boards in one unit, and molded. Each of these classifications, except for molded, can be further subdivided into single-sided, double-sided, or multilayer PWBs.

The circuit interconnection pattern, except for molded PWBs, is created by imaging the conductor pattern on copper sheets using a photoresist material and one of two image-transfer techniques—screen printing or photo imaging. The resist acts as a protective cover defining the conductor patterns while unwanted copper is etched away. Molded PWBs are usually nonplanar (three-dimensional) and consist of conductive materials selectively applied through printing conductive pastes or additively plating conductors to either extruded or injection molded thermoplastic resins.

These techniques can be used with a variety of dielectric materials to achieve various mechanical and electrical characteristics in the final product. Among the most common dielectric materials are epoxy/e-glass (electronic-grade glass) laminates used in the fabrication of rigid PWBs and polyimide film used in the fabrication of flexible printed wiring. The rigid-flex boards use a combination of these two materials.

22.2.1.1 Rigid PWB

The rigid PWB is fabricated from copper-clad dielectric materials. The dielectric consists of an organic resin reinforced with fibers. The most commonly used fiber materials are paper and e-glass. The organic media can be of a wide formulation and include flame-retardant phenolic, epoxy, polyfunctional epoxy, or polyimide resins.

As the name implies, rigid PWBs consist of layers of the organic laminates that are laminated through heat and pressure into a rigid interconnection structure. This structure is usually sufficiently rigid in nature to be able to support the components that are mounted to it. Specialized applications may require the PWB to be mounted to a support structure. The support structure may be used to remove heat generated by the components, decrease the movement of the PWB under extreme vibration.

The rigid PWB interconnection structure may be further subdivided by the number of wiring layers contained within the structure into the following three categories—single-sided, double-sided, or multilayered. Figure 22.1 shows a cross-sectional view of each type.

Single-Sided PWBs: A single-sided PWB consists of a single layer of copper inter-connection (usually on the component side of the PWB). The rigid dielectric material is fabricated from multiple layers of unclad laminate material pressed to the final end-use thickness. A single layer of copper cladding is applied to one of the outside layers during this process. In some instances double-sided copper cladding may be used, with the copper on one face being completely etched away during the processing.

The base laminate of single-sided boards can be of woven or paper (unwoven) materials with copper foil, usually of 1- or 2-oz weight, clad to one side. It should be noted here that copper cladding is most often referred to by its weight (1 oz/ft^2 equals 0.00137 in thick) rather than by its thickness. The raw clad laminate is first cut into working panels suited to the equipment, which will handle the subsequent operations. The panel is then drilled or punched to provide a registration system. Laminate flatness is important in achieving a good registration baseline. These are critical in an automated print and etch system because the panel tends to warp after the copper is removed during etching. This warping allows stresses built into the material during its fabrication to be relieved. Excessively warped panels may not register properly for subsequent operations.

The individual artworks which define the conductor patterns are then arranged or panelized so that one or more PWBs will be produced from a single panel. This is accomplished by stepping and repeating the patterns into a panel phototool. Once the panel layout is established, the panel can be drilled or punched to produce the final hole pattern. Holes required are either drilled in glass-reinforced products or punched in paper-reinforced products. Registration of the conductor pattern to holes is accomplished through either the right-angle edge of the panel or on pilot holes contained in opposite comers of the panel. Drilling of holes is usually done after the panels are first cut; punching of holes is done as the last operation.

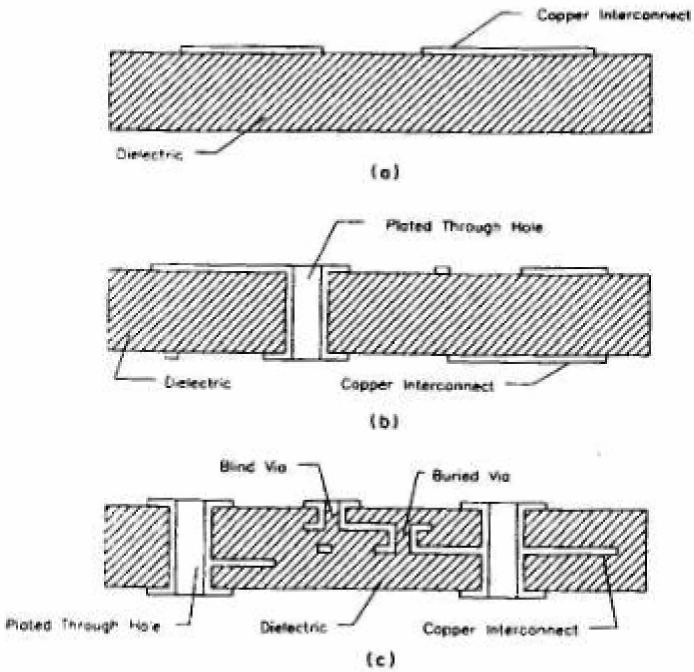

Figure 22.1 Organic PWBs (a) single-sided, (b) double-sided, and (c) multilayer

Following the drilling operation, the etch resist is applied and the circuit pattern formed. This pattern can be made by printing a liquid resist or photo imaging of a film or liquid. The next step is to etch away the unwanted copper from the laminate, leaving only the desired circuit pattern. Finally the resist is stripped and the single-sided board is complete in panel form.

At this point additional processes such as platings or solder masks may be performed, or the individual boards may be sheared or routed from the panel.

While single-sided boards with their simplicity might seem doomed due to the emergence of modern complex electronics, they continue to have a substantial market, especially where cost is a strong driver. Their use with fairly complex IC devices can be seen in many places, such as watches, cameras, and automobiles. This will probably continue to be the case for the foreseeable future.

Double-Sided PWBs: From a historical perspective the double-sided board is probably the most often designed type of all PWBs. It retains much of the production simplicity of the single-sided board but allows circuit complexities far in excess of 2:1 over its simpler cousin. This is the case because it allows basic x and y routing of the circuit on its two outer faces, thus improving the routing efficiency and the circuit density. Interconnection of the two conductor patterns is accomplished through drilling and subsequent plating or filling the interconnection holes, called vias. The most widely used method is to plate the vias with copper. Silver-conductive ink is another process used in low-cost consumer products.

Double-sided boards are fabricated from laminates with copper (usually 1 oz) clad to both outside layers. The copper may be clad to a variety of materials. Here, as with the single-sided board, the material is purchased from a laminator who specializes in providing laminates to the electronic industry.

Once the raw laminate is cut into panels, the fabrication operation begins with the inter-connection hole drilling. The via holes may also serve as mounting holes for the components to be soldered into. After the via hole pattern has been drilled, the holes may be filled with the conductive ink or the panel is copper plated by an electroless technique in preparation for subsequent plating by either of two methods—pattern plating or panel plating.
The conductor image is formed in a similar way as with single-sided boards, except that the photoresist application and imaging take place on both sides of the panel. Obviously, the registration of the photo images from one side of the panel to the other is critical. The circuit pattern on one side must be properly registered to the pattern on the other side, or the plated-through holes will not properly connect between the two sides.

The next step is to etch away the copper laminate, leaving only the desired circuit pattern. At this point additional processes such as resist stripping, platings, or solder masks may be performed and the individual PWBs then sheared or routed from the panel (see Fig. 22.1).

Multilayered PWBs. Multilayer boards are those PWBs having three or more conductive layers, including any pads-only layers. The typical modern multilayer board will have from 4 to 10 layers of circuitry, with some high-density applications requiring upward of 50 layers. Most multilayer boards are fabricated by laminating single- or double-clad, pre-etched, patterned sheets of thin (<0.005-in) laminate together using partially cured resin in a carrier fabric. The materials commonly used for this purpose are discussed at length in Section22.3.

The single- or double-clad laminate material is processed similarly to the single- or double-sided PWB, except that the via or component holes are usually not drilled until after lamination. It should be noted here that the importance of registration is amplified as the layer count increases. Increased pad sizes may be required to minimize via hole breakout due to misregistration. The same requirement may limit the size of panels due to run out of the circuit features.

Following the fabrication of the individual layers or layer pair, a "book" of layers and their interposed bonding layers are stacked together in a particular sequence to achieve the required lay-up. This book is then laminated under heat and pressure to the appropriate thickness for the final board. The outer layers are not pre-etched so that the laminated book appears the same as a double-sided copper-clad laminate of comparable thickness. After lamination, the book is processed the same as a thick double-sided board. The book is drilled to add the via holes and then processed as if it were a double-sided board using plated-through holes. A cross-section of a typical multilayer board is shown in Fig. 22.1.

In some cases standardized layers, such as power or ground distribution can be "mass"-laminated into the raw laminate. This is a very cost-effective means of achieving multilayer density at near double-sided board cost since the outer layer processing and via drilling is identical to that for double-sided PWB processing. As a result, four-layer boards are the most prevalent multilayer boards.

Where circuit density requirements override cost considerations, techniques such as blind or buried vias are used to increase the interconnection wiring density on a given layer. Where these techniques are used, the inner layer pairs are fabricated as double-sided boards, complete with plated vias, and then assembled into books for processing into multilayer boards. Thus the inner layers may be interconnected without a via hole through the entire board. Similarly, blind vias may connect to the first or subsequent buried layer on each side of the board without penetrating the entire board (see Figure 22.1).

The multilayer board has now achieved a cost and reliability level that allows its use in any level of electronics. It is no longer the exclusive tool of the mainframe computer, telecommunications, or military electronics. It is often seen even in toys.

22.2.1.2 Flexible PWB

As defined by the Institute for Interconnection and Packaging Electronic Circuits (IPC), flexible printed wiring is a random arrangement of printed wiring, Utilizing flexible base material with or without cover layers. Interconnection systems consisting of flat cables, collated cable, ribbon cable and sometimes wiring harnesses are sometimes confused with flexible printed wiring. Flexible printed wiring is used in applications requiring continuous or periodic movement of the circuit as part of the end product function and those applications where the wiring cannot be planar and is moved only for servicing. Flexible wiring can be used as interconnect cabling harnesses between various systems circuit card assemblies and or connectors as well as to interconnect individual electrical components. Figure 22.2 shows a typical flexible printed wiring interconnect.

Visually, flexible printed wiring looks similar to rigid printed wiring. The main difference in the products is the base or dielectric material. Flexible printed wiring is manufactured using ductile copper foil bonded to thin, flexible dielectrics. The dielectric materials include polyimide (Kapton), polyester terephthalate (Mylar), random fiber aramid (Nomex), polyamide-imide TFE Teflon and FEP Teflon and polyvinyl chloride (PVC).

As with their rigid printed wiring, the flexible printed wiring may be manufactured in single-sided, double-sided or multilayer configurations as shown in Figure 22.3. The conductor patterns are formed in a similar manner to rigid PWBs using either a screen printing or photo-imaging of a resist to form the conductor pattern and then etching of the unwanted copper. A variety of adhesive materials are used in their manufacture to bond the various layers together. These including acrylics, epoxies, phenolic butyrals, polyesters, and polytetrafluoroethylene (PTFE). In addition, newer processes have been developed to laminate the conductor directly to the dielectric film without the use of an adhesive layer.

On single- and double-sided flexible wiring, cover layers are often used to protect the etched copper circuitry. When a film cover layer is employed, the access holes to the circuitry are either punched or drilled in the adhesive-coated film. The cover layer is then mechanically aligned to the wiring and laminated in a platen press under heat and pressure. The adhesive systems must be of a "no" or "low" flow formulation to keep from contaminating the interconnection pads. Screen printable cover coats may also be used. These are usually ultraviolet curable and give a moderately pinhole-free insulating surface.

Unlike their rigid counterparts, the outline features of flexible wiring are not routed but cut using either soft or hard tooling. Soft tooling involves a rule die. In its simplest form, this can be a steel die and Exact to knife to cut the outline pattern. More complex dies may consist of steel strips imbedded in plywood. When pressed against the flexible wiring they act as cookie cutters to form the outline. Rule dies are dimensionally less accurate and less expensive than hard tools. Hard tools are punches, die plates and strippers manufactured from hardened steel. They can hold tolerances within the die of ±0.001 in.

Figure 22.2 Typical flexible printed wiring interconnect in connector assembly

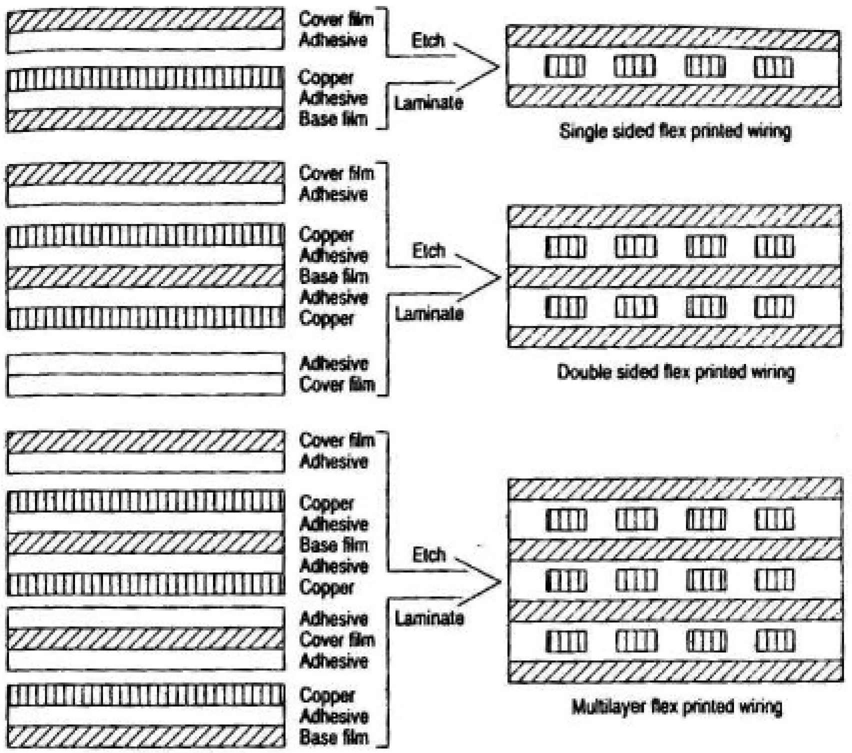

Figure 22.3 Flexible PWB types

Due to the extreme flimsiness of flexible wiring, when components are to be mounted, adequate reinforcement must be added to the flexible wiring to eliminate stress points at the component circuit interfaces. Reinforcements typically used are simple pieces of unclad rigid laminates or complex formed, cast or machined metals or plastics to which the flexible wiring is laminated.

22.2.1.3 Rigid-Flexible

Rigid-flex circuitry consists of single or multiple flexible wiring layers selectively bonded together using cither a modified acrylic adhesive or an epoxy bond film. Cap layers of rigid core copper clad laminate may be bonded to the top and bottom surfaces of the circuit to add further stability to the bonded areas as shown in Figure 22.4(a).

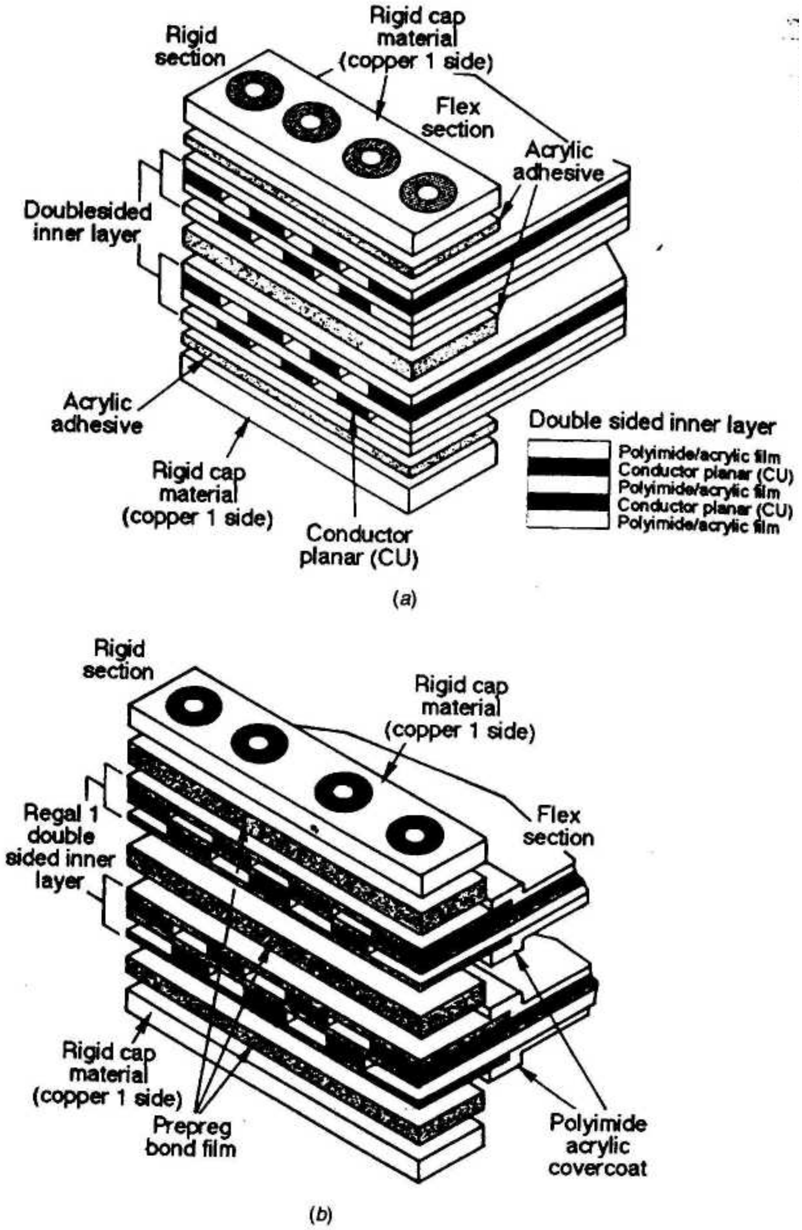

Figure 22.4(a) Rigid-flexible multilayer, (b) REGAL flexible multilayer

To allow for increased reliability in multilayer applications, the amount of acrylic adhesive in the rigidized area must be limited. There are a couple of methods in use in the IP industry today to accomplish this. One method involves using a polyimide/acrylic base with a cover coat in the rigid area and a polyimide acrylic selective cover coat in the flexible areas. This technique does force the manufacturer to develop tooling techniques to overlap the separate dielectrics.

A second technique that was developed is called a Rigid Epoxy Glass Acrylic Laminate (REGAL) Flex as shown in Figure 22.4(b). In this technique, the manufacturer starts with a base stock of Epoxy prepreg clad with copper. The traces are etched in the copper. The base-stock epoxy prepreg is then encapsulated in the flex area with flexible dielectric to allow the circuit to bend. The traces in the rigid section are encapsulated with epoxy prepreg which has been windowed to remove the prepreg from the flex section. Each cover coated flex layer can be selectively bonded together with pre-windowed epoxy prepreg to form a rigidized area for subsequent through hole processing.

The benefits of rigid-flexible wiring are apparent in the design, manufacturing, installation and assembly, quality control and product enhancement of the end item.

The designer has increased conceptual freedom in the end item design. Conformability, three dimensional interconnects and a space saving form factor are benefits. In many cases reduced interconnect length lead to optimal electrical performance. Mechanical and electrical interfaces are reduced and mechanical, thermal and electrical characteristics are more repeatable than with conventionally wired systems.

In manufacturing their use leads to reduced assembly costs within a totally unitized interconnect system. There are increased opportunities for automation. In addition, reduced system interconnect errors and improved system interconnect yields occur.

Installation and assembly benefits include elimination of miswiring and indexing errors encountered in discrete wired systems. A reduction in the installer skill and training, increased speed of installation and mounting simplification leading to reduced hardware requirements are other benefits.

Quality control benefits by the adaptability of the product to automated inspection, a simplification of error cause analysis and more effective error cause correction.

Products are enhanced through a reduced weight, volume and cost. Fewer interconnections are usually required leading to increased system reliability. Reduction in product inventory, maintenance and field service time and expense are also realized.

22.2.2 Ceramic PWBs

These PWBs are classified by their method of manufacture and type of metallization. There are four distinct types. Thick film uses alumina, beryllia, and similar materials as the substrate base material and fired thick-film dielectric paste (a glass-frit paste) as the dielectric. Conductors are formed from fired conductive noble metal pastes. Thin film uses ceramic, glass, quartz, silicon, or sapphire as the substrate base and deposits various metals by plating, sputtering, or vapor deposition. Cofired substrates can be broken into two distinct groupings. Cofired ceramic uses ceramic tape as the dielectric that is cofired with refractory metal pastes which form the conductors; cofired low-temperature tape uses a glass/ceramic tape dielectric that is cofired with noble metal pastes which form the conductors. Direct-bond copper directly bonds copper conductors to a ceramic substrate. All of these ceramic-based PWBs are most often referred to as substrates.

Ceramic boards do offer advantages, compared to organic boards. The ceramic dielectric is inherently much more rigid than organic material dielectrics. Component soldering (183 to 240 °C) is usually performed above or near the glass transition temperature T_g of organic materials (100 to 240 °C) and can lead to damaged PWBs when the process is controlled improperly. The 1600 °C needed to fire ceramic is well above this soldering temperature.

Higher thermal conductivities available with ceramic materials offer improved thermal management over organic boards. When thermal vias are required, the smaller buried vias available with ceramic boards provides a low thermal resistance while sacrificing less routing area.

Increased costs and design time are disadvantages to the use of ceramic boards. A weight penalty is usually paid when ceramic boards are used. The ceramic and noble metal materials used in ceramic boards are also more costly than their organic counterparts. The demand for these boards has usually been in low-volume military and avionics applications. This has led to a limited number of ceramic PWB facilities, which has also helped to maintain higher costs. The following sections describe in detail each of the four different ceramic substrate types.

22.2.2.1 Thick Film

This class of ceramic PWBs is manufactured by building up alternating layers of conductors and dielectric on a ceramic substrate. A thick-film substrate may be called a true printed circuit in that resistive elements may also be built into the substrate. Thick-film substrates have dielectric thicknesses of 0.0015 to 0.0025 in, metallization thicknesses of 0.0005 to 0.001 in, and resistor thicknesses of 0.001 to 0.0015 in. Each layer is pattern-printed onto the substrate using screen or stencil printing processes.

Several different ceramic materials can be used as the substrate base. These include alumina, beryllia, aluminum nitride, boron nitride, silicon carbide, and silicon nit depending on the end item requirements. Dielectric, conductor, and resistive inks (pastes) are printed and fired to build the interconnect structure.

The manufacture of a thick-film ceramic PWB begins with the generation of artwork defining the following: conductor patterns, dielectric layers including via openings in multilayer applications, via fill patterns, and resistor networks when required. From this artwork a screen or stencil for each wiring, via, resistor, and dielectric layer is developed. When a screen is to be used, its manufacturing begins with stainless-steel wire mesh stretched over a metal frame. Nylon and polyester mesh are sometimes used due to their lower costs. They can stretch and be affected by temperature and humidity and are not as durable as the stainless-steel screens. The mesh count (number of wires per linear in screen) and wire diameter determine the obtainable print resolution of the various layers. In general, mesh counts vary from 200 to 400 and wire diameters from 0.9 to 1.1 mil, with the lower mesh counts (200) and greater wire diameters (1.1 mil) being used for gross conductor patterns (>0.010-in line widths and spaces).

A photosensitive polyvinyl or polyimide emulsion is next applied to the screen, and the conductor, dielectric, via, or resistor pattern is photo-imaged on the emulsion under ultraviolet light using the artwork. Uncured resin is then washed away, leaving the final conductor pattern. The emulsion thickness determines the final wet print thickness of the various layers for a given mesh and wire diameter.

Stencil printing involves etching the patterns to be printed in a thin metal foil, usually nickel or brass. This once again uses photoresistive materials in a photpimaging operation to define the pattern and then etching away the unwanted metal similar to etching copper on a PWB laminate. The metal stencil is then mounted in a metal frame. The advantages of stencils over screen meshes are many. They offer more uniform print thicknesses, greater print resolution, reduced dimensioning capabilities, and easier process control.

The ceramic substrate is prepared by cutting to size using laser drilling, diamond scribing, or ultrasonic milling. The laser is by far the most prevalent method. Overlapping of the laser drill hole pattern can yield a smooth cut surface. Spacing of the holes yields a perforated surface, which can be used to define a number of substrates on a single ceramic panel. This "snapstrate" can be processed, and after the processing is completed, the individual substrates can be snapped along the perforation.

Cleaning of the ceramic to remove the melted ceramic or glass residue (slag) left after laser drill is called deslagging. A variety of methods may be used, including sandblasting with alumina slurry followed by a cleaning in hot isopropyl alcohol. Subsequent heating in a furnace at 800 to 925 °C is usually done to burn off any organic contaminants left during the previous processes.

Following substrate preparation, the metallization process begins. Conductive, dielectric, or resistive inks (pastes) contain the desired metals or conductors. These are combined with glass frits to allow bonding during firing and needed solvents to accomplish a definable print. Each layer is printed, dried to volatilize the solvents, and then fired in a furnace. This print, dry, fire sequence continues until the multilayer structure is complete. Resistor layers are the last high-temperature firing (800 to 900 °C) performed and are done together. Subsequent high firings can cause an oxidation of the resistive material and an unacceptable rise in resistance of the material. A low-temperature (425 to 525 °C) glass encapsulant can be printed and fired over selective resistors and conductors as a protective overcoat or solder mask. Resistors are usually trimmed to a final value using a laser-trimming process. This requires the overcoat encapsulant to be composed of a glass that allows the laser to penetrate to the resistor.

Thick-film ceramic boards are used mainly as interconnect substrates in multichip modules. Their use as interconnection substrates for applications similar to rigid organic PWBs is usually limited to a maximum PWB size of 8 in.

22.2.2.2 Thin Film

Thin-film ceramic boards are normally limited to specialized designs or single-layer applications. They are more expensive and difficult to multilayer when compared to their thick-film counterparts. Their use requires the substrate surface to be very flat and smooth and causes higher-purity ceramics to be used. These include alumina, glass, quartz, silicon, or sapphire. Thin-film metallizations use noble metals (such as gold) and are used most often in microwave applications due to their improved electrical performance over thick-film substrates at higher frequencies.

Thin-film interconnections in multilayer applications are through buried vias, as is the case with all ceramic PWBs. The top and bottom metallization on a double-sided substrate can be connected using plated-through holes for electrical interconnection or improved thermal performance. Metallization patterning of thin-film ceramics is accomplished through the use of photo lithography, plating, etching, vapor deposition, and sputtering methods.

22.2.2.3 Cofired

This type of ceramic PWB requires the printing of pastes containing conductor metallization onto unfired tape (dielectric) materials. These layers are then stacked and cofired together in a furnace to form the interconnect structure. The unfired tape materials can be either ceramic or a low-temperature dielectric.

The ceramic tape system requires higher firing temperatures. This results in refractory metals such as tungsten, molybdenum, or tungsten copper to be used as the conductor within the paste. These metals have higher vaporization temperatures to withstand the firing, but lower thermal and electrical conductivities than the noble metals (gold, silver, or copper). Their lower conductivities typically limit the use of these substrates to digital applications.

The conductor paste is applied to the tape using a screen or stencil similar to the thick-film process. For multilayer applications, holes are punched in the dielectric prior to printing. The conductive paste fills the hole and later forms a buried via during the firing operation. After all layers have been printed, they are stacked in the proper sequence, laminated together under heat and pressure, and fired to solidify the ceramic.

Upon completion of the cofiring operation, the exposed refractory metals are electroplated with typically 0.000080 to 0.000350 in of nickel and 0.000050 to 0.000100 in of gold. The nickel acts as a barrier to intermetallic formations between the gold and tungsten and as a corrosion barrier. The gold serves as a wire-bondable or solderable surface for component attachment.

The dielectric tape systems are composed of lower-temperature reflow glasses similar to those found in thick-film pastes. The printing, stacking, and laminating operations fare the same as those used for the ceramic materials. The firing, however, occurs at a lower firing temperature, which allows the use of noble metal pastes. These tapes allow the substrates to be used in microwave applications. In addition, no additional platings are required upon postfiring.

Cofired PWBs offer distinct advantages over thin- or thick-film processed PWBs. Multilayering is limited only by the thickness limitation of the overall package. Each fired layer is 0.003 to 0.012 in thick, depending on the tape thickness used. Thermal vias may be more readily incorporated into the design using an array of vias punched in the dielectric and filled with conductive pastes. Cutting of the tape prior to stacking and firing can allow cavities to be formed in the final product to allow component mounting. Cofired substrates are the main manufacturing method used to produce leadless chip carrier and multichip module component bodies. The patterning of the conductor layers prior to firing allows for easier inspection and rework.

The main disadvantages are in the longer life-cycle time needed to develop the tooling required to produce the item.

22.2.2.4 Direct-Bond Copper

As the name implies, a direct-bond copper (DBCu) board uses copper directly bonded to a ceramic dielectric. The most commonly used ceramic is alumina, although beryllia and aluminum nitride (which offer improved thermal performance) have been used successfully in the process. The DBCu structure offers improved thermal and structural performance compared with conventional thick- or thin-film technologies using alumina dielectrics.

The process involves oxidation of the surface of a copper foil, which is then placed against a ceramic substrate. The pieces are placed in a furnace which reflows the copper oxide and fuses it with the surface ceramic oxides. This directly bonds the two materials together.

Any currently available ceramic material thicknesses can be used (0.005 to 0.125 in). Copper foils of 0.001- to 0.080-in thickness have been used successfully. To prevent the substrate from warping or cracking, it is recommended that the copper foil thickness be less than or equal to the ceramic thickness.

The bonding process occurs at approximately 1000 °C. During cooling, the copper contracts at a much higher rate than the ceramic. The cooling increases the tensile strength of the ceramic by an order of magnitude by placing it in compression. This allows thinner ceramic materials to be used and will decrease the overall assembly height and reduce the thermal resistance of the board. Coupling the reduction in thickness with the heat-spreading capabilities of copper allows a DBCu board to offer reductions in thermal resistance.

The copper interconnect features can be formed by punching the copper sheet prior to attachment to the ceramic or by photo-imaging techniques similar to those used in rigid PWBs after bonding to the ceramic. The latter process allows finer line features. Typically, 0.015-in minimum line widths and spacings are used.

Alternately stacking layers of copper and ceramic can create multilayer interconnect structures. Three conductor layers are the limits achieved to date. Buried vias consisting of windows in the ceramic filled with copper spheres or particles are used to interconnect from layer to layer.

DBCu boards offer the advantages of improved structural strength, thermal management, and high thermal conductivity. In addition, the copper offers bondability when nickel- or gold-plated and is capable of excellent solderability. Limitations in dimensioning and multilayering are its disadvantages.

22.2.3 Developmental PWBs

Advances in the state of the art of integrated circuitry are leading to systems applications requiring higher packaging densities and improved thermal and electrical performance. In many instances this has led to the requirement for multichip modules to be designed to meet system electrical throughput and volumetric requirements. This has placed increasing emphasis on the interconnection substrate design within the module. Ceramic materials with their high dielectric constant impart unacceptable losses in throughput due to propagation delay for high-speed applications. In addition, limitations in wiring density on the substrate due to the printing techniques used cause unacceptably thick substrates because of the need for more wiring layers. New combinations of standard materials and processes have been combined to address these requirements. These are mainly in the form of a thin-film dielectric on silicon or ceramic.

The dielectric used by most companies is polyimide. A thin-film polyimide layer is applied through screen printing or spinning onto a silicon or ceramic substrate. In some instances the silicon or ceramic may have wiring routed within. The polyimide is then metallized with aluminum or copper and patterned using standard thin-film photo-imaging techniques. Via interconnects from layer to layer are done in an additive "pillar" process. The polyimide dielectric layers provide a thin, low-dielectric-constant material (<4.0), and the thin-film metallization allows very-high-density routing (0.001- to 0.002-in lines and spaces).

A second interconnection technique involving a thin-film polyimide process involves the "growing" of a circuit on top of the die in a multichip module. This technique, called high-density interconnect (HDI), was developed by General Electric. Here, die are mounted into wells inside a multichip package (MCP) such that the top of the die forms a planar surface with the inside surface of the module. Polyimide dielectric and thin-film metal layers are then fabricated on top of the die to perform the interconnection.

Another developing technology for multichip module applications is the silicon circuit board (as shown in Figures. 22.5and 22.6). This board uses silicon as a base substrate. The difference in this board over similar silicon interconnection techniques is the use of silicon dioxide as the dielectric material instead of polyimide. The manufacturer reports that material costs less as a base material and requires fewer processing steps than polyimide. It offers a second advantage in that a thin silicon dioxide layer between power and ground planes in the substrate gives an integral decoupling capacitor between the planes not obtainable with other technologies.

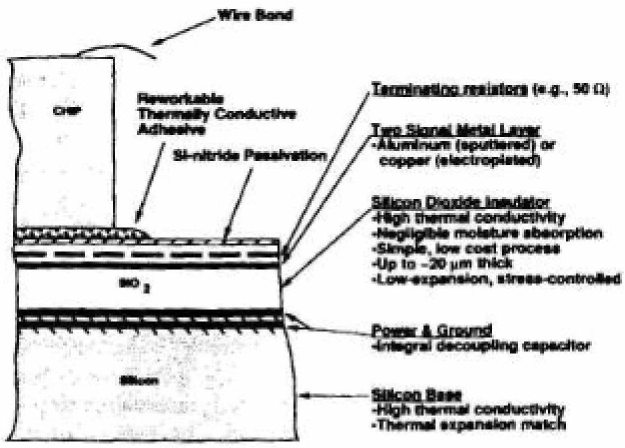

Figure 22.5 Cross-sectional view of silicon circuit board

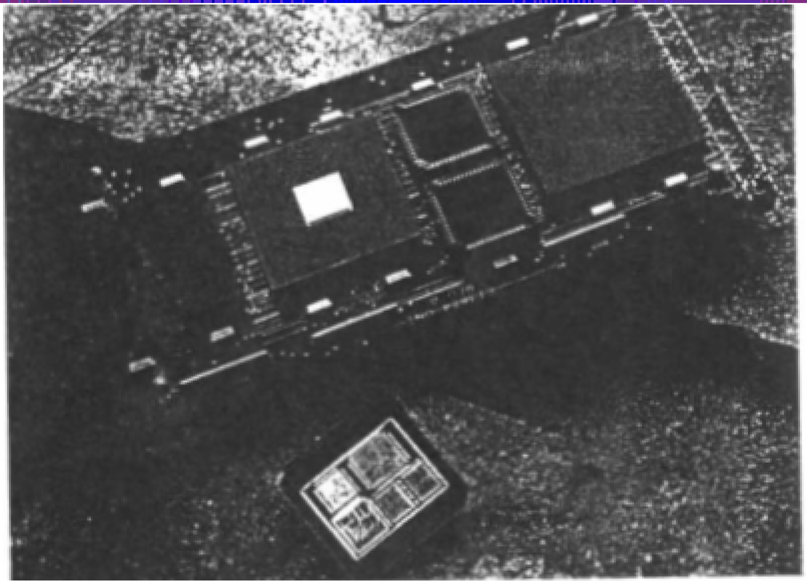

Figure 22.6.High-speed RISC/SPARC processor using multichip design with silicon circuit board

22.2.4 Discrete-Wired PWBs

Most discrete-wired boards use an organic rigid PWB as a base substrate, their primary difference being that the circuit is wired using discrete or individual wires. Several varieties of theses boards are in use today. Such as the multiwire board, the Microwire board, the stitch –welded board and the wire-wrap technique. Lets to discuss the multiwire board only into considered.

22.2.4.1 Multiwire

Multiwire technology was developed as an alternative PWB method to conventional multilayer PWBs. The invention of Multiwire addressed a variety of concerns of multilayer PWB designers and fabricators. The time and cost required to produce the artwork films (especially for existing designs, which need to be quickly modified), layer-to-layer registration requirements of a large number of layers, and the inability to inspect or repair inner layers in a finished product are reduced or eliminated using this technology.

Multiwire most commonly uses a rigid epoxy/e-glass laminate as a base, although any base material (polyimide, metal core, or flexible material) used in the printed-circuit industry can be used.

The design of the wiring is done on a computer-assisted design (CAD) system. The CAD system generates the necessary instructions to drive a numerically controlled wiring machine. Wiring can be done in an x-y orthogonal grid as well as at a 45° angle to intersect the component locations as shown in Figure. 22.7.

After all wires have been routed, they are pressed more deeply into the adhesive and then encapsulated with an epoxy cover and copper foil. The board at this stage resembles a conventional multilayer PWB prior to the drilling step.

A via pattern is drilled at the component locations using conventional drilling processes, which cut into the wiring. The holes are cleaned using high-pressure water and prepared for copper plating in a proprietary alkaline permanganate solution.

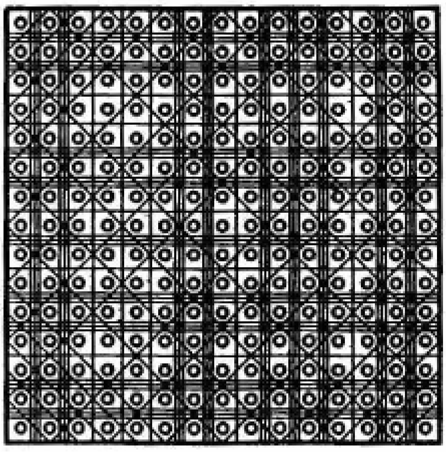

Figure 22.7 Multiwire typical wired circuit pattern using x-y and 45° geometry

This solution removes resin smear and microetches the hole wall to promote plating adhesion. In addition, it chemically removes some of the wire insulation at the point of wire entry into the drilled hole.

Hole plating to complete the interconnect is accomplished in a way similar to conventional PWB processing. The boards are catalyzed and plated using an appropriate electro-less copper bath. Application of a dry-film photoresist defines the surface features. Exposed holes and surface features are then electroplated with copper and then tin-lead plated. The photoresist is stripped and the tin-lead plate acts as the resist for etching the background copper and completing the termination process. Figure 22.8 describes the final structure of a Multiwire board.

It should be noted that the Multiwire board use is aimed toward through-hole component (such as DIP and PGA) designs and low-density SMT designs. To address ultra-high-density SMT designs another product, called Microwire.

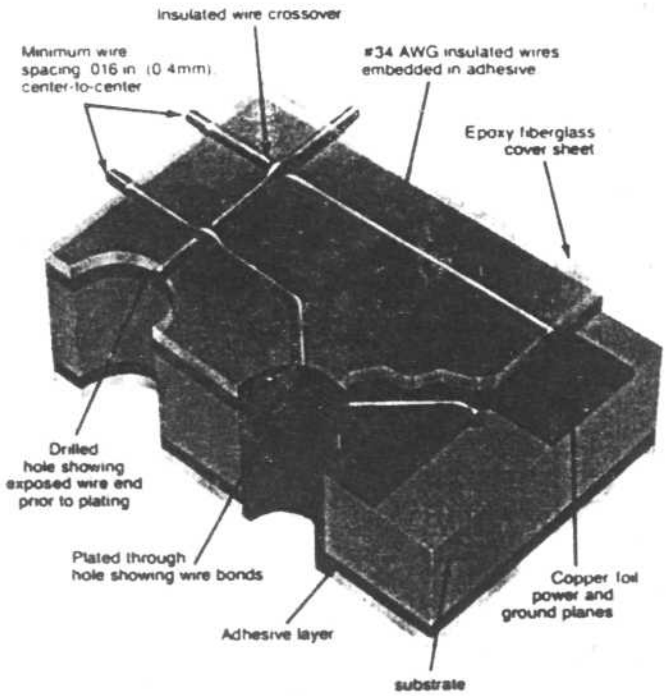

Figure 22.8 Cross-sectional view of typical multiwire board

22.3 Conformal Coatings for PWB Assemblies

Conformal coatings have been used for many years. Their main functions have been to protect circuit boards from dust, dirt, and moisture.

In the past due to the cost of the coating itself as well as the cost of applying the coating to the board, only the most expensive boards or those with especially demanding needs for reliability were coated (mainly military). With advances in application technology and process ability the economics of using conformal coatings have improved favorably.

Additionally as circuit size has diminished and components have become more delicate the need for a protective coating has become a necessity in many cases.
The different Conformal Coatings for PWB are described as follow.

22.3.1 Acrylic Coatings

Acrylics are excellent coating systems from a production standpoint because they are relatively easy to apply. Furthermore, application mistakes can be corrected readily, because the cured film can be removed by soaking the printed circuit assembly in a chlorinated solvent such as trichloroethane or methylene chloride. Spot removal of the coating from isolated areas to replace a component can also be accomplished easily by saturating a cloth with a chlorinated solvent and gently soaking the area until the cured film is dissolved.

Since most acrylic films are formed by solvent evaporation, their application is simple and is easily adaptable to manufacturing processes. Also, they reach optimum physical characteristics during cure in minutes instead of hours.

Acrylic films have desirable electrical and physical properties, and they are fungus-resistant. Further advantages include long pot life, which permits a wide choice of application procedures; low or no exotherm during cure, which avoids damage to heat-sensitive components; and no shrinkage during cure. The most obvious disadvantage of the acrylics is poor solvent resistance, especially to chlorinated solvents.

22.3.2 Polyurethane Coatings

Polyurethane coatings are available as either single- or two-component systems. They offer excellent humidity and chemical resistance and good dielectric properties for extended periods of time.

In some instances the chemical resistance property is a major drawback because rework becomes more costly and difficult. To repair or replace a component, a stripper compound must be used to remove effectively all traces of the film. Extreme caution must be exercised when the strippers are used, because any residue from the stripper may corrode metallic surfaces.

In addition to the rework problem, possible instability or reversion of the cured film to a liquid state under high humidity and temperature is another phenomenon which might be a consideration. However, polyurethane compounds are available to eliminate that problem.

Although polyurethane coatings systems can be soldered through, the end result usually involves a slightly brownish residue which could affect the aesthetics of the board. Care in surface preparation is most important, because a minute quantity of moisture on the substrate could produce severe blistering under humid conditions. Blisters, in turn, lead to electrical failures and make costly rework mandatory.

Single-component polyurethanes, although fairly easy to apply, require anywhere from 3 to 10 days at room temperature to reach optimum properties. Two-component polyurethanes, on the other hand, provide optimum cure at elevated temperatures within 1 to 3 h and usually have working pot lives of 30 min to 3 h.

22.3.3 Epoxy Coatings

Epoxy systems are available, as two-component compounds only, for coating electronic systems. Epoxy coatings provide good humidity resistance and high abrasive and chemical resistance. They are virtually impossible to remove chemically for rework, because any stripper that will attack the coating will also attack epoxy-coating or potted components and the epoxy-glass printed board as well. That means that the only effective way to repair a board or replace a component is to burn through the epoxy coating with a knife or soldering iron.

When epoxy is applied, a buffer material must be used around fragile components to prevent fracturing from shrinkage during the polymerization process. Curing of epoxy systems can be accomplished either in 1 to 3 h at elevated temperature or in 4 to 7 days at room temperature. Since epoxies are two-component materials, a short pot life creates an additional limitation in their use.

22.3.4 Silicone Coatings

Silicone coatings are especially useful for high-temperature service (approximately 200°C). The coatings provide high humidity and corrosion resistance along with good thermal endurance, which makes them highly desirable for PWAs that contain high heat-dissipating components such as power resistors.

Repairability, which is a prime prerequisite in conformal coating, is difficult with silicones. Because silicone resins are not soluble and do not vaporize with the heat of a soldering iron, mechanical removal is the only effective way to approach spot repair. That means the cured film must be cut away to remove or rework a component or assembly. In spite of some limitations, silicone coatings fill a real need because they are among the few coating systems capable of withstanding temperatures of 200 °C.

22.3.5 Polyimide Coatings

Polyimide coating compounds provide high-temperature resistance and also excellent humidity and chemical resistance over extended periods of time. Their superior humidity resistance and thermal range qualities are offset by the need for high-temperature cure (from 1 to 3 h at 200 to 250 °C). High cure temperatures limit the use of these coating systems on most printed circuit assemblies. Because the polyimides were designed for high-temperature and chemical resistance, chemical removal and burn-through soldering cannot be successful.

22.3.6 Silicon Nitride Coating

Silicon Nitride has been in use as a passivation coating on integrated circuits since the early 1970s. With the advent of chip on board (COB) packaging for use in both military and harsh consumer environments, this coating has begun to be looked at as a conformal coating for board level COB applications. A room temperature plasma deposition system has been developed by Ionic Systems that allows a low stress silicon nitride coating to be applied over components on a circuit assembly. The silicon nitride coating thickness is approximately 0.5 μm.