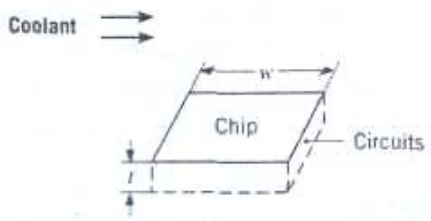
Part G-3: Solved Problems

1. A square silicon chip (k = 150 W/m. K) is of width w =5 mm on a side and of thickness t = 1 mm. The chip is mounted in a substrate such that its side and back surfaces are insulated, while the front surface is exposed to a coolant. If 4 W are being dissipated in circuits mounted to the back surface of the chip, what is the steady-state temperature difference between back and front surfaces?



Data given: Chip dimensions, its thermal conductivity, and 4 W input power to the chip from the back surface of the chip.
Require: Temperature difference across the chip.
Assumptions:

(a) Steady-state conductions.
(b) Constant properties.
(c) One-dimensional conduction in the chip.
(d) Neglect heat loss from back and sides.

Solution:
From Fourier's law,

$$q = -kA\frac{dT}{dx}$$

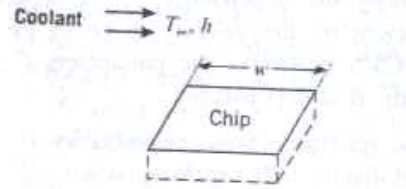
Or,

$$P = q = kA\frac{\Delta T}{t}$$

Then,

$$\Delta T = \frac{tP}{kA} = \frac{0.001 \text{ X } 4}{150 \text{ X } (0.005)^2} = 1.07 \ ^oC$$

2. A square isothermal chip is of width w = 5 mm on a side and is mounted in a substrate such that its side and back surfaces are well insulated, while the front surface is exposed to the flow of a coolant at T_∞ = 15 °C. From reliability considerations, the chip temperature must not exceed T = 85 °C.
If the coolant is air and the corresponding convection coefficient is h = 200 W/m^2 K. What is the maximum allowable chip power? If the coolant is a dielectric liquid for which h = 3000 W/m^2.K. What is the maximum allowable power?



Data given: Chip width, coolant conditions, and maximum allowable chip temperature.
Require: maximum allowable chip power at air and dielectric liquid.
Assumptions:

(a) Steady-state conditions.
(b) Neglect heat loss from back surface and sides.
(c) Neglect the heat transferred by radiation.
(d) Chip is at uniform temperature (isothermal).

Solution:
According to Newton's law,

$$q = hA(T_s - T_\infty) = P$$

For air cooling,

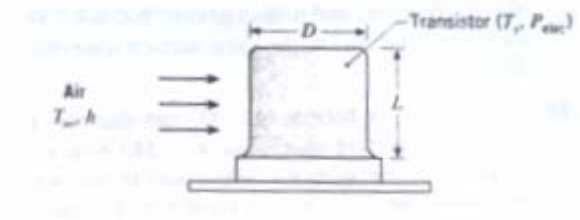
$$P_{\max} = hA(T_{s,\max} - T_\infty) = 200 \text{ X } (0.005)^2 \text{ X } (85-15) = 0.35\,W$$

For dielectric liquid cooling,

$$P_{\max} = hA(T_{s,\max} - T_\infty) = 3000 \text{ X } (0.005)^2 \text{ X } (85-15) = 5.25\,W$$

Comment: at comparison between both air and liquid cooling. It appears the air heat transfer is poorer than the liquid heat transfer but cooling with liquid is higher cost.

3. The case of a power transistor, which is of length L = 10mm and diameter D = 12 mm, is cooled by an air stream of temperature T_∞ = 25 °C. Under conditions for which the air maintains an average convection coefficient of h = 100 W/m^2.K on the surface of the case, what is the maximum allowable power dissipation if the surface temperature is not to exceed 85 °C?



Data given: transistor dimensions, air coolant conditions, and maximum allowable chip temperature.

Require: maximum allowable transistor power.
Assumptions:

(a) Steady-state conditions.
(b) Neglect heat loss from base, and top surfaces.
(c) Neglect the heat transferred by radiation.
(d) Transistor is at uniform temperature (isothermal).

Solution:
According to Newton's law,

$$q = hA(T_s - T_\infty) = P$$

According to the maximum surface transistor temperature, the maximum allowable transistor power is,

$$P_{\max} = hA(T_{s,\max} - T_\infty) = 100 \text{ X } (\pi \text{ X } 0.012 \text{ X} 0.01) \text{ X } (85 - 25) = 2.262\ W$$

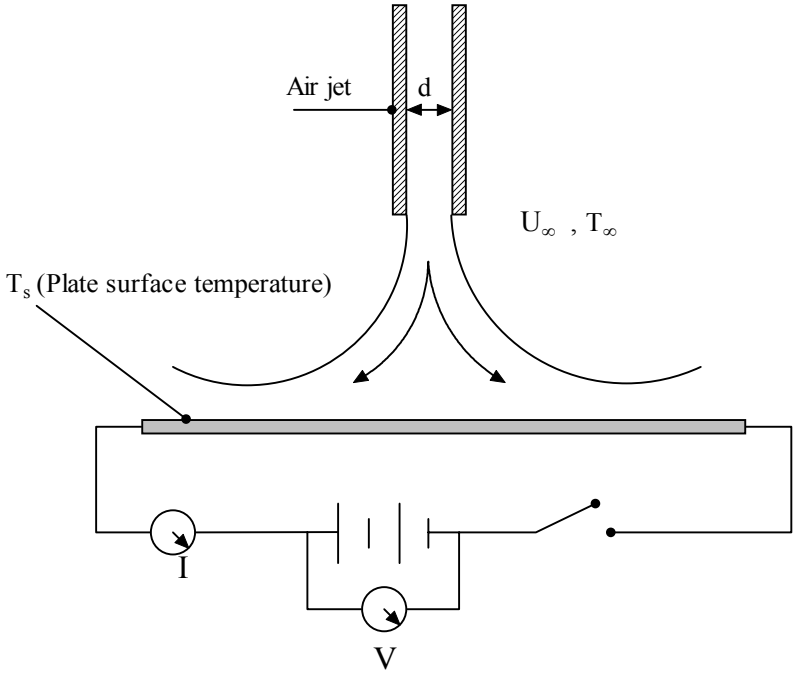
4. The use of impinging air jets is proposed as a means of effectively cooling high-power logic chips in a computer. However, before the technique can be implemented, the convection coefficient associated with jet impingement on a chip surface must be known. Design an experiment that could be used to determine convection coefficients associated with air jet impingement on a chip measuring approximately 10 mm by 10 mm on a side.

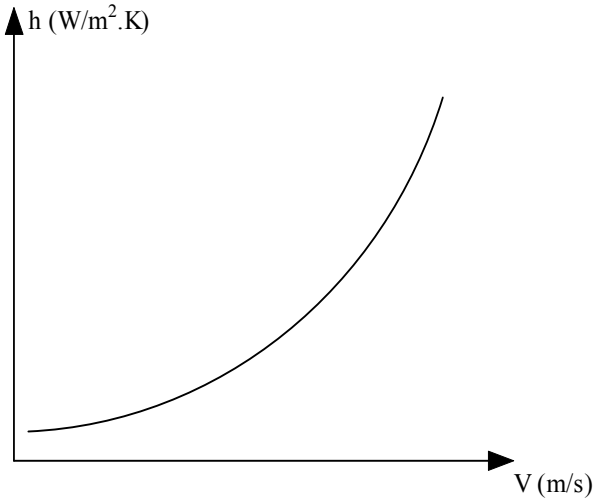
Given data: chip dimensions.
Required: determine the convection heat transfer coefficients experimentally.
Solution:
We will give the experiment in steps as follow,

1) Construct the system including its components as shown in figure below.
2) Bring voltmeter to measure the electric potential volt.
3) Bring ammeter to measure the electric current.
4) Bring thermometer to measure the surface temperature.
5) Close the electric circuit key.
6) Let constant power supply (IV = const.), plate surface area (A = const.), and free stream air temperature (T_∞ = const.).
7) The heat transfer coefficient depends on Reynolds number, and Prandtl number. Then by changing the jet air velocities according to its flow rates it will gives different heat transfer coefficients, which obtained according to the following relation, by known each measured plate surface temperature T_s (varied with each jet air velocity)..

$$q = IV = hA(T_s - T_\infty)$$

8) Plot the relation between the jet air velocities and heat transfer coefficients.





The suggested out put chart: Shows the effect of jet air velocities on heat transfer coefficients.

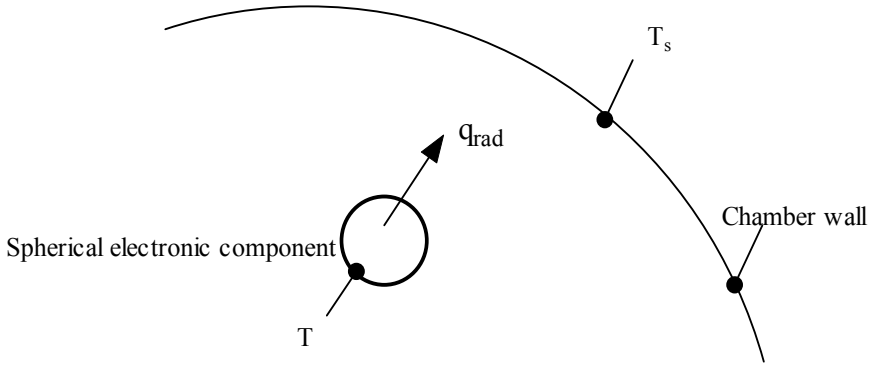
5. An instrumentation package has a spherical outer surface of diameter D = 100 mm and emissivity ε = 0.25. The package is placed in a large space simulation chamber whose walls are maintained at 77 K. If operation of the electronic components is restricted to the temperature range $40 \leq T \leq 85$ °C, what is the range of acceptable power dissipation for the package? Display your results graphically, showing also the effect of variations in the emissivity by considering values of 0.20 and 0.30.

Given data: Instrumentation emissivities (ε) and its surface temperature range $40 \leq T \leq 85$ °C
Require: The range of acceptable power dissipation for the package
Assumptions:

(a) Steady-state conditions.

(b) The chamber is very large compared to package size.
(c) Constant chamber wall temperature is maintained at 77 K.
(d) The chamber is evacuated.

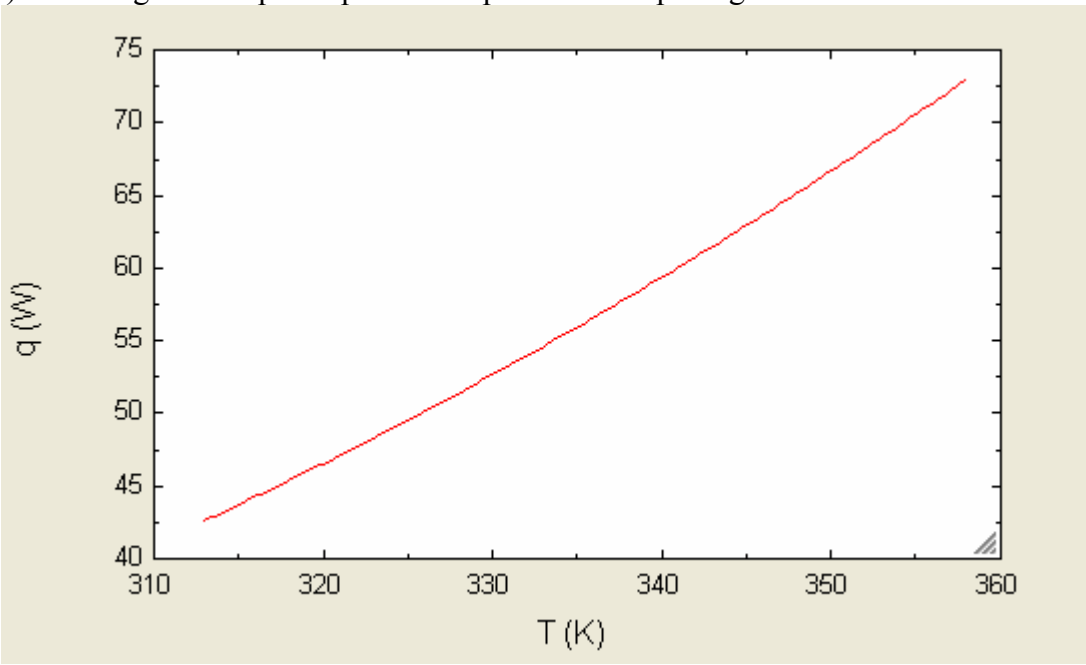
Solution:



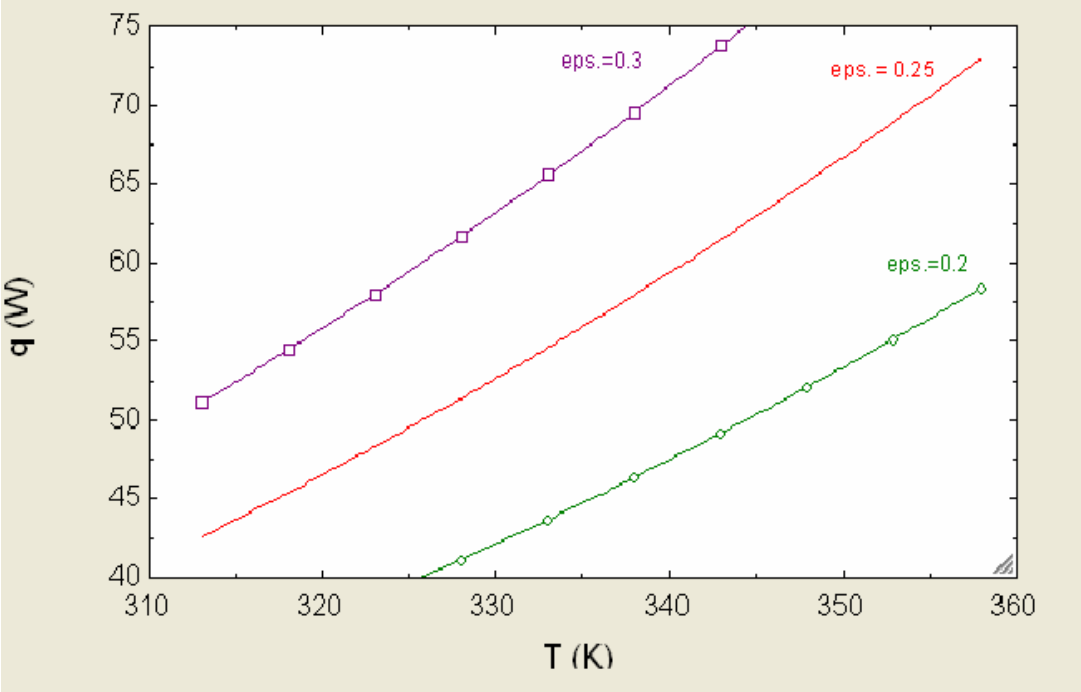
Because the electronic component in a large enclosure then the geometrical factor $f = 1$. Then the radiation heat transfer from the electronic component to the chamber wall is:

$$q = \sigma\varepsilon\, fA(T^4 - T_s^4)$$
$$= 5.67 \text{ X } 10^{-8} \text{ X } \varepsilon \text{ X } 1 \text{ X } (\pi \text{ X } 0.1^2)(T^4 - 77^4)$$
$$= 1.7813 \text{ X } 10^{-8}\ \varepsilon\ (T^4 - 77^4)$$

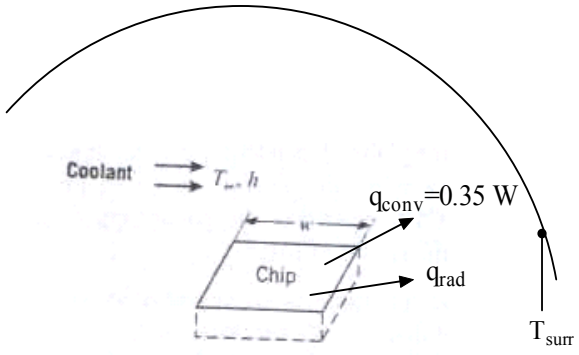
1) The range of acceptable power dissipation for the package at ε = 0.25



2) The effect of variations in the emissivity



6. Consider the conditions of Problem 2. With heat transfer by convection to air, the maximum allowable chip power is found to be 0.35 W. If consideration is also given to net heat transfer by radiation from the chip surface to large surroundings at 15 °C, what is the percentage increase in the maximum allowable chip power afforded by this consideration?
The chip surface has an emissivity of 0.9.



Data given: Chip width, coolant conditions, and maximum allowable chip power due to convective air cooling, maximum allowable chip temperature, and large surroundings temperature.
Require: percentage increase in the maximum allowable chip power due to radiation effect.
Assumptions:
(a) Steady-state conditions.
(b) Radiation exchange between small surface and large enclosure.
(c) Chip is at uniform temperature (isothermal).

Solution:
The radiation heat transfer is

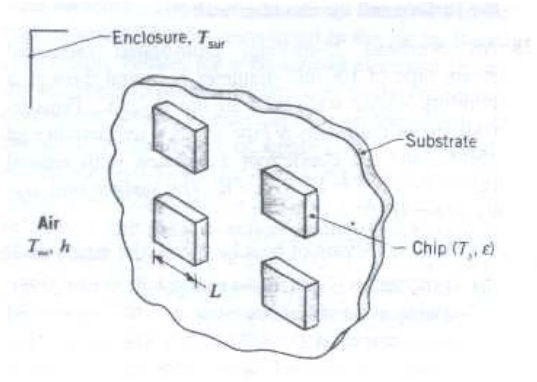
$$q = \sigma\varepsilon\, fA(T^4 - T_{surr}^4)$$
$$= 5.67 \text{ X } 10^{-8} \text{ X } 0.9 \text{ X } 1 \text{ X } (0.005)^2 (358^4 - 288^4)$$
$$= 0.0122\, W$$

Percentage increase in chip power due to radiation effect is

$$\%P_{\max} = ((0.35 + 0.0122)/0.35) - 1) * 100 = 3.49\ \%$$

7. A square chips of width L = 15 mm on a side are mounted to a substrate that is installed in an enclosure whose walls and air are maintained at a temperature of $T_\infty = T_{surr} = 25$ °C. The chips have an emissivity of $\varepsilon = 0.60$ and a maximum allowable temperature of $T_s = 85$ °C.

(a) If heat is rejected from the chips by radiation and natural convection, what is the maximum operating power of each chip? The convection coefficient depends on the chip-to-air temperature difference and may be approximated as $h = C (T_s - T_\infty)^{0.25}$, Where C = 4.2 $W/m^2.K^{5/4}$.
(b) If a fan is used to maintain air flow through the enclosure and heat transfer is by forced convection, with h = 250 $W/m^2.K$, what is the maximum operating power?



Given data: Chip width, walls and air temperatures, the chip emissivity, and maximum allowable chip temperature.

Require:
(a) Maximum operating power of each chip.
(b) Maximum operating power if a fan is used and heat transfer is by forced convection, with h = 250 W/m^2.

Assumptions:
(a) Steady-state conditions.
(b) Chip is at uniform temperature (isothermal).

(c) Radiation exchange between small surface and large enclosure.

Solution:

(a) The maximum operating chip power is the summation of heat transfer due to convection and radiation is

$$P_{\max} = q_{tot} = q_{conv} + q_{rad}$$
$$= hA(T_s - T_\infty) + \sigma\varepsilon fA(T_s^4 - T_{surr}^4)$$
$$= 4.2(0.015)^2(85-25)^{1.25} + 5.67\ \text{X}\ 10^{-8}\ \text{X}\ 0.6\ \text{X}\ 1\ \text{X}(0.015)^2(358^4 - 298^4)$$
$$= 0.2232\ W$$

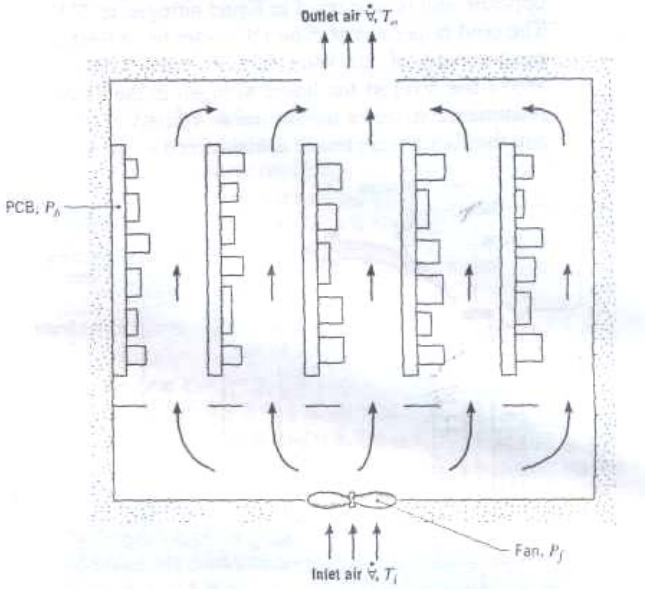
(b) Maximum operating power if a fan used is

$$P_{\max} = q_{tot} = q_{conv} + q_{rad}$$
$$= hA(T_s - T_\infty) + \sigma\varepsilon fA(T_s^4 - T_{surr}^4)$$
$$= 250(0.015)^2(85-25) + 5.67\ \text{X}\ 10^{-8}\ \text{X}\ 0.6\ \text{X}\ 1\ \text{X}(0.015)^2(358^4 - 298^4)$$
$$= 3.44\ W$$

8. A computer consists of an array of five printed circuit boards (PCBs). Each dissipating P_b = 20 W of power. Cooling of the electronic components on a board is provided by the forced flow of air, equally distributed in passages formed by adjoining boards, and the convection coefficient associated with heat transfer from the components to the air is approximately h = 200 W/m^2.K. Air enters the computer console at a temperature of T_i = 20 °C, and flow is driven by a fan whose power consumption is P_f =25 W.

(a) If the temperature rise of the air flow. (T_o - T_i), is not to exceed 15 °C, what is the minimum allowable volumetric flow rate of the air? The density and specific heat of the air may be approximated as ρ= 1.161kg/m^3 and C_p = 1007J/kg.K, respectively.

(b) The component that is most susceptible to thermal failure dissipates 1 W/cm^2 of surface area. To minimize the potential for thermal failure, where should the component be installed on a PCB? What is its surface temperature at this location?



Given data: Five printed circuit boards (PCBs) each dissipating P_b = 20 W of power, convection coefficient associated with heat transfer from the components to the air, Air inlet temperature, and fan power consumption.

Assumptions:

(a) Steady-state conditions.
(b) Neglect the heat transferred by radiation.

Solution:

(a) By overall energy balance on the system including fan power is

$$5P_b + P_f = \dot{m}_a C_p (T_o - T_i)$$

$$5 \text{ X } 20 + 25 = 1.161 \text{ X } \dot{V}_a \text{ X } 1007(15)$$

The total volumetric flow rate of the air is

$$\dot{V}_a = 0.00713\ m^3/s$$

(b) To minimize the potential for thermal failure, the component should be installed on a PCB at the coolest air condition which at air entrance.

The board air inlet temperature which equals to temperature leaving the fan is

$$T_{b,i} = (P_f / \dot{m}_a C_p) + T_i$$

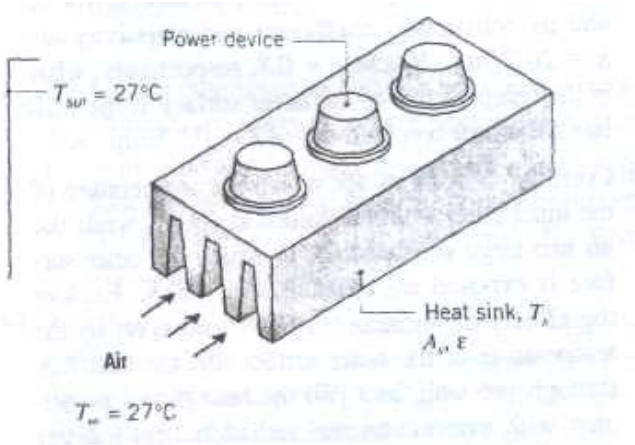
$$= (25/1.161\text{X}0.00713\text{X}1007) + 20 = 23\ ^oC$$

The heat flux occurs at maximum temperature difference.

$$q'' = h\Delta T_{\max} = h(T_s - T_{b,i})$$
$$10000 = 200(T_s - 23)$$

The surface temperature at this location T_s equals 73 ^{o}C.

9. Electronic power devices are mounted to a heat sink having an exposed surface area of 0.045 m^2 and an emissivity of 0.80. When the devices dissipate a total power of 20 W and the air and surroundings are at 27 °C, the average sink temperature is 42 ^{o}C. What average temperature will the heat sink reach when the devices dissipate 30 W for the same environmental condition?



Given data: heat sink surface area, the average sink temperature and its emissivity, total power dissipation, air and surrounding temperatures

Require: Sink temperature when dissipation is 30 W.

Assumptions:

(a) Steady-state conditions.
(b) All dissipated power in devices transferred to the sink.
(c) Sink is at uniform temperature (isothermal).
(d) Radiation exchange between small surface (heat sink) and large enclosure (surrounding) case.
(e) Convective coefficient is the same for both power levels.

Solution:

At a total power device of 20 W.

$$P = q_{tot} = q_{conv} + q_{rad}$$
$$= hA(T_s - T_\infty) + \sigma\varepsilon fA(T_s^4 - T_{surr}^4)$$
$$20 = 0.045h(42 - 27) + 5.67 \text{ X } 10^{-8} \text{ X } 0.8 \text{ X } 1 \text{ X} 0.045(315^4 - 300^4)$$

The convective heat transfer coefficient h is

$$h = 24.35\, W/m^2.K$$

When the devices dissipate 30 W. Using the same value of heat transfer coefficient.

$$30 = 0.045 \text{ X } 24.35(T_s - 300) + 5.67 \text{ X } 10^{-8} \text{ X } 0.8 \text{ X } 1 \text{ X} 0.045(T_s^4 - 300^4)$$

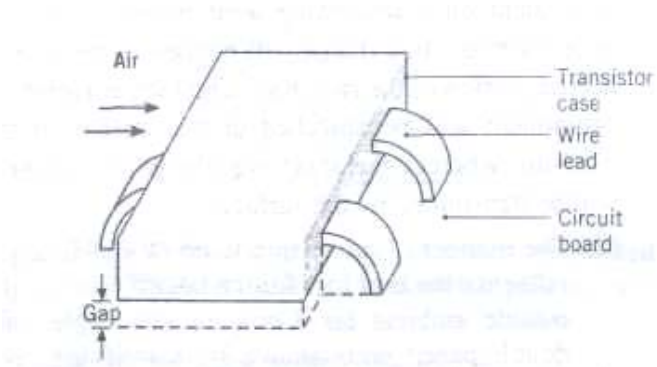
By trial-and-error, the temperature of the heat sink is

$$T_s = 322 \text{ K} = 49\ ^{o}\text{C}$$

10. Consider a surface-mount type transistor on a circuit board whose temperature is maintained at 35 °C. Air at 20 °C flows over the upper surface of dimensions 4 mm by 8 mm with a convection coefficient of 50 W/m^2.K.Three wire leads, each of cross section 1 mm by 0.25 mm and length 4 mm, conduct heat from the case to the circuit board. The gap between the case and the board is 0.2 mm.

(a) Assuming the case is isothermal and neglecting radiation; estimate the case temperature when 150 mW are dissipated by the transistor and (i) stagnant air or (ii) a conductive paste fills the gap. The thermal conductivities of the wire leads, air. And conductive pastes are 25, 0.0263, and 0.12 W/m.K. respectively.

(b) Using the conductive paste to fill the gap, we wish to determine the extent to which increased heat dissipation may be accommodated, subject to the constraint that the case temperature not exceeds 40 °C. Options include increasing the air speed to achieve a larger convection coefficient h and/or changing the lead wire material to one of larger thermal conductivity. Independently considering leads fabricated from materials with thermal conductivities of 200 and 400 W/m.K, compute and plot the maximum allowable heat dissipation for variations in h over the range $50 \leq h \leq 250$ W/m^2.K.



Given data: Surface-mount transistor, power dissipation by conduction and convection

Required:

(a) The case temperature with (i) air-gap and (ii) conductive paste fills the gap.

Assumptions:

(a) Steady-state conductions.
(b) Constant properties.
(c) Transistor case is isothermal.

(d) One-dimensional conduction.
(e) Neglect heat loss from edges.

Solution:
By energy balance across the transistor case

$$P = 3q_{lead} + q_{conv} + q_{cond,gap}$$

$$q_{lead} = k_l A_l (T_c - T_b) / L$$

Where T_c is the case temperature, and T_b is the board temperature

$$q_{conv} = hA_c (T_c - T_\infty)$$

$$q_{cond,gap} = k_g A_g (T_c - T_b) / \delta_{gap}$$

Substitute in the energy equation:

$$P = 3k_l A_l (T_c - T_b) / L + hA_c (T_c - T_\infty) + k_g A_g (T_c - T_b) / \delta_{gap}$$

(i) By substitute in numerical values for air-gap condition

$$0.15 = \left[3(25)(0.001\text{X}0.00025) / 0.004 + 0.0263(0.008\text{X}0.004) / 0.0002\right](T_c - 35) + 50(0.008\text{X}0.004)(T_c - 20)$$

The case temperature with air-gap is

$$T_c = 47\ ^oC$$

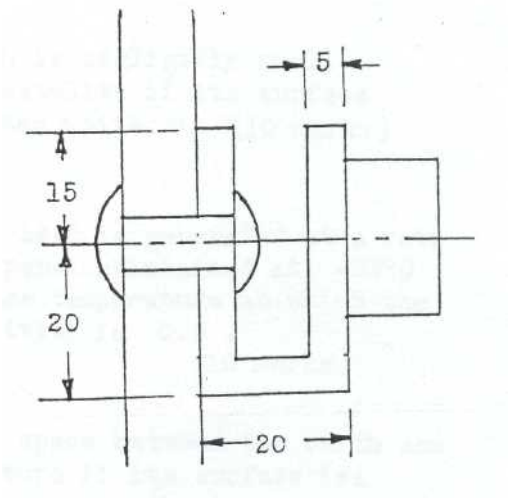
(ii) By substitute in numerical values for conductive paste fills the gap condition

$$0.15 = \left[3(25)(0.001\text{X}0.00025) / 0.004 + 0.12(0.008\text{X}0.004) / 0.0002\right](T_c - 35) + 50(0.008\text{X}0.004)(T_c - 20)$$

The case temperature with conductive paste fills the gap is

$$T_c = 40\ ^oC$$

11. A transistor that dissipates10W is mounted on a duralumin heat sink at 50 °C by a duralumin bracket 20 mm wide as shown in the opposite figure. The bracket is attached to the heat sink by a rivet. With convective cooling negligibly small, estimate the surface temperature of the transistor.



Given data: Transistor power dissipation, and heat sink temperature and bracket dimensions
Require: Surface temperature of the transistor.
Assumptions:

(a) Neglect the convection cooling.
(b) Neglect the contact resistances
(c) One-dimension conduction.
(d) Steady state condition.

Solution:

The heat source is the base of the transistor and the rivets connecting the bracket to the heat sink,
The heat flow path length is

$$L = 20 + 20 + 20 = 60 \text{ mm}$$

The base transistor area equals the heat flow area is

$$A = \text{width x thickness} = 20 \text{ x } 5 = 100 \text{ mm}^2$$

The duralumin thermal conductivity could be obtained from appendix is

$$k = 164 \text{ W/m.K}$$

From Fourier's law,

$$P = q = kA\frac{\Delta T}{L}$$

Then the surface temperature of the transistor is

$$T_s = 50 + (10 \text{ X } 0.06)/(164 \text{ X } 100 \text{ X } 10^{-6}) = 86.58 \ ^oC$$

Comment: Essentially in this case, conduction is not one-dimensional conduction. But the solution based on one-dimensional conduction only for simplicity with loss of accuracy.

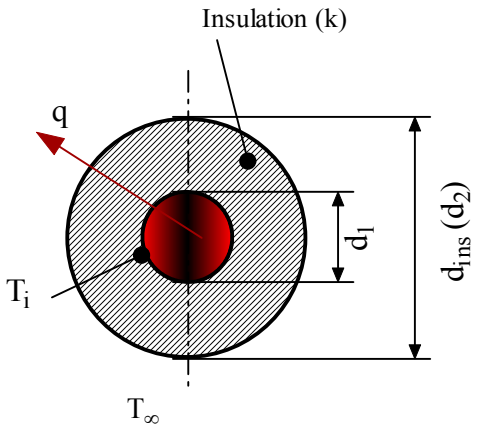
12. A cable 10 mm diameter is to be insulated to maximize its current carrying capacity. For certain reasons, the outside diameter of the insulation should be 30 mm. The heat transfer coefficient for the outer surface is estimated to be 10 W /m^2 .K.
What should be the thermal conductivity of the chosen insulation? By what percentage would the insulation increase the energy carrying capacity of the bare cable?

Given data: Cable diameter, insulation diameter and heat transfer coefficient.

Require: thermal conductivity of insulation required to maximize the current carrying capacity, and the percentage increase in the energy carrying capacity due to insulation.

Assumption:
(a) One-dimensional conduction.
(b) Steady-state conditions

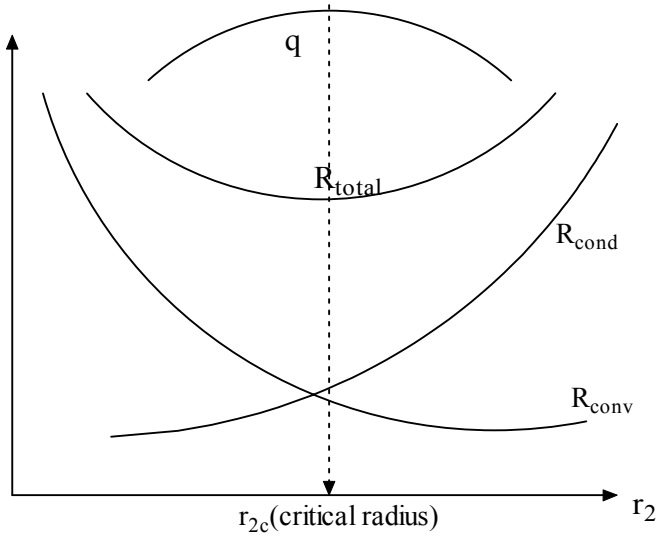
Solution:



The heat transfer from the cable is

$$q = \frac{\Delta T}{\sum R_{th}} = \frac{T_i - T_\infty}{R_{cond} + R_{conv}} = \frac{T_i - T_\infty}{\ln\left(\frac{r_2}{r_1}\right)/(2\pi kL) + \left(\frac{1}{h(2\pi r_2 L)}\right)}$$

For increasing the radius of insulation the conduction resistance increases, on another hand the convection resistance decreases. So that there's a minimum total thermal resistance causes maximum heat transfer (or current carrying capacity) as shown.



To find the maximum heat transfer: differentiate the heat transfer to the radius of insulation (r_2). Then equal it to zero. It gives

$$r_{2c} = \frac{k}{h}$$

At h = 10 W /m^2 .K. and r_{2c} = 0.015 m

The thermal conductivity of insulation required to maximize the current carrying capacity is

$$k = 0.015 \text{ x } 10 = 0.15 \text{ W /m .K.}$$

$$q'_{\max} = \frac{\Delta T}{\ln\left(\frac{r_{2c}}{r_1}\right)/(2\pi k) + \left(\frac{1}{h(2\pi r_{2c})}\right)} = \frac{\Delta T}{\ln(15/5)/(2\pi \text{ X } 0.15) + \left(\frac{1}{10(2\pi \text{ X } 0.015)}\right)} = \Delta T / 2.2267 \text{ W/m}$$

For bare cable the heat transfer is

$$q'_{bare} = \frac{\Delta T}{\left(\frac{1}{h(2\pi r_1)}\right)} = \frac{\Delta T}{\left(\frac{1}{10(2\pi \text{ X } 0.005)}\right)} = \Delta T / 3.183 \text{ W/m}$$

The percentage increase in the energy carrying capacity due to insulation is

$$\% \, q_{increase} = \{(q'_{\max} / q'_{bare}) - 1\} 100 = 43 \, \%$$

13. The vertical side of an electronics box is 40 x 30 cm with the 40 cm side vertical. What is the maximum radiation energy that could be dissipated by this side if its temperature is not to exceed 60 °C in an environment of 40 °C, and its emissivity is 0.8?

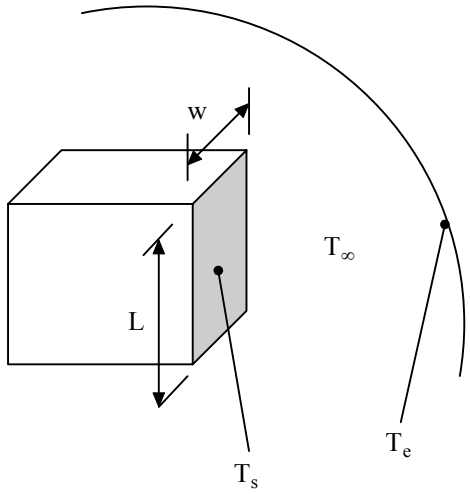
Given data: electronics box vertical side area, maximum temperature of the electronics box vertical side, its emissivity, and the environment temperature.

Require: maximum radiation energy dissipates from this side of the electronic box

Assumptions:

(a) Steady-state conditions.
(b) Radiation exchange between small surface and large enclosure.
(c) The side is at uniform temperature (isothermal).
(d) The temperature of the enclosure equals the temperature of the environment.

Solution:



The maximum radiation energy dissipates from this side of the electronic box is

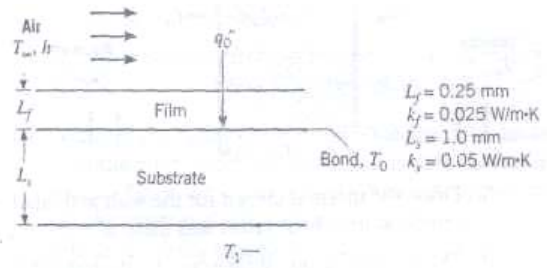
$$q_{\max} = \sigma\varepsilon f A(T_s^4 - T_e^4)$$
$$= 5.67 \text{ X } 10^{-8} \text{ X } 0.8 \text{ X } 1 \text{ X}(0.4 \text{ X } 0.3)(333^4 - 313^4)$$
$$= 14.7\ W$$

14. In a manufacturing process, a transparent film is being bonded to a substrate as shown in the sketch. To cure the bond at a temperature T_o, a radiant source is used to provide a heat flux q_o'' (W/m^2), All of which is absorbed at the bonded surface. The back of the substrate is maintained at T_1 while the free surface of the film is exposed to air at T_∞ and a convection heat transfer coefficient h.

(a) Show the thermal circuit representing the steady-state heat transfer situation. Be sure to label all elements, nodes, and heat rates. Leave in symbolic form.

(b) Assume the following conditions: T_∞ = 20 °C, h = 50 W/m^2.K and T_1 = 30 °C. Calculate the heat flux q_o'' that is required to maintain the boded surface at T_o = 60 °C.

(c) Compute and plot the required heat flux as a function of the film thickness for $0 \le L_f \le 1$mm.



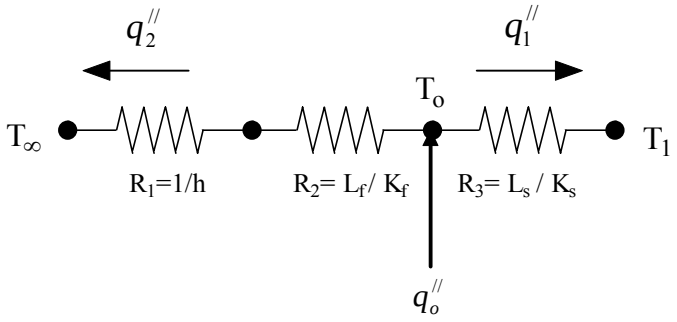
Given data: A radiant source is used to provide a heat flux at the bond to cure the bond at a temperature T_o.

Assumptions:

(a) Steady-state conditions.
(b) Constant properties.
(c) One-dimensional conduction heat transfer.
(d) Neglect the contact resistance.

Solution:

(a) Thermal circuit based on heat flux distribution represented below.



(b) Using this thermal circuit and performing energy balance on film-substrate interface,

$$q_o'' = q_1'' + q_2''$$

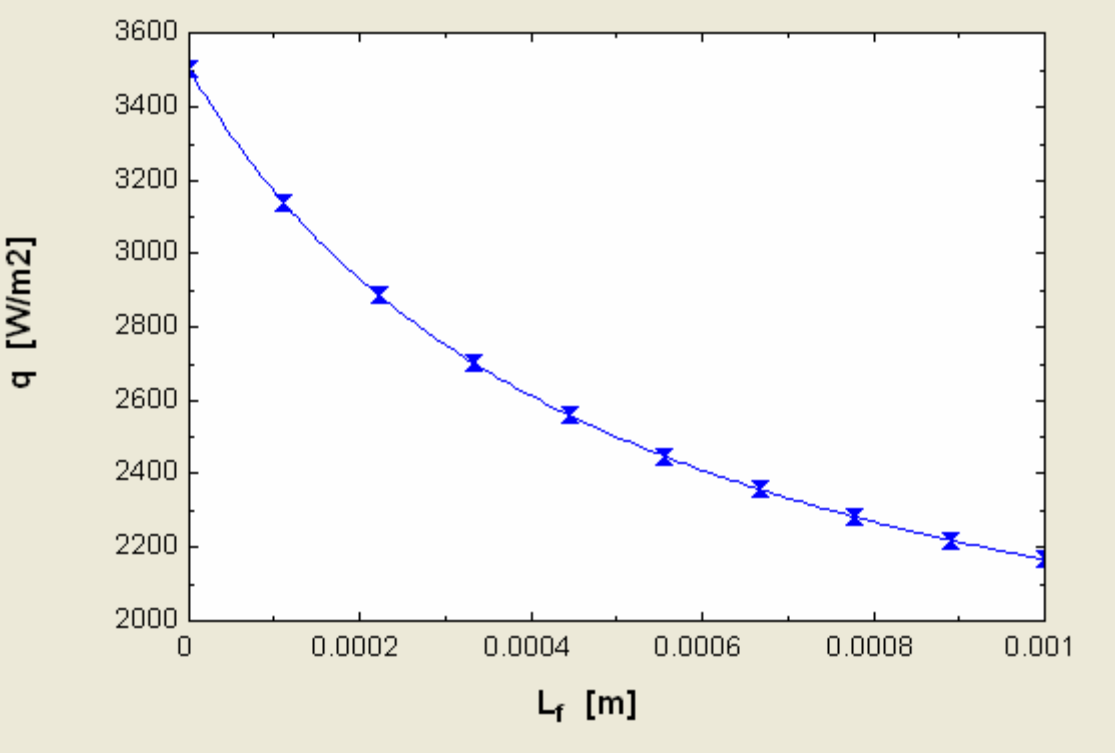
$$= \frac{(T_o - T_1)}{(L_s / k_s)} + \frac{(T_o - T_\infty)}{(L_f / k_f) + (1/h)}$$

$$= \frac{60 - 30}{(0.001/0.05)} + \frac{60 - 20}{(0.00025/0.025) + (1/50)}$$

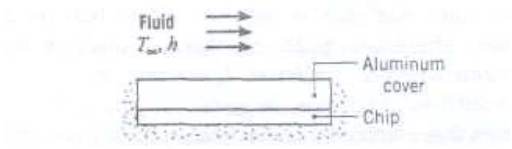
$$= 2833 \text{ W/m}^2$$

(c) The heat flux as a function of the film thickness,

$$q_o'' = q_1'' + q_2''$$
$$= \frac{(T_o - T_1)}{(L_s / k_s)} + \frac{(T_o - T_\infty)}{(L_f / k_f) + (1/h)}$$
$$= 1500 + \frac{40}{40\,L_f + 0.02} \quad \text{W/m}^2$$



15. A silicon chip is encapsulated such that, under steady-state conditions, all of the power it dissipates is transferred by convection to a fluid stream for which h = 1000 W/m^2.K and T_∞ = 25 °C. The chip is separated from the fluid by a 2-mm-thick aluminum cover plate, and the contact resistance of the chip/aluminum interface is 0.5 x 10^{-4} m^2.K/W. If the chip surface area is 100 mm^2 and its maximum allowable temperature is 85 ^{o}C, what is the maximum allowable power dissipation in the chip?

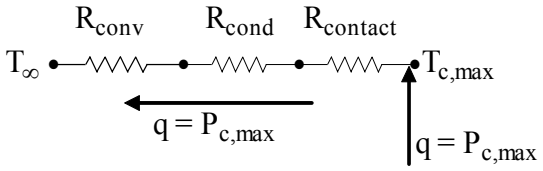


Given data: chip surface area is 100 mm^2 and its maximum allowable temperature, contact resistance of the chip/aluminum interface and fluid stream conditions.
Require: maximum allowable power dissipation in the chip.
Assumption:

(a) Steady-state conditions

(b) Neglect the radiation heat transfer.
(c) One-dimensional conduction.
(d) Neglect the heat loss from the back and side surfaces.
(e) Chip at uniform temperature (isothermal).

Solution:
The thermal circuit of the system represented as shown in the following figure, Conduction heat transfer from the chip equals the convection heat transfer to the fluid stream,



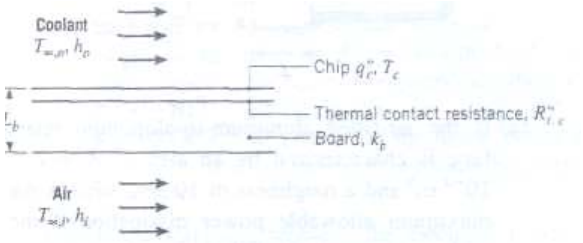
According to the thermal circuit, the maximum allowable power dissipation in the chip is

$$q = P_{c,\max} = \frac{T_{c,\max} - T_\infty}{R_{contact} + R_{cond} + R_{conv}} = \frac{T_{c,\max} - T_\infty}{(1/hA)_{contact} + (L/KA)_{Alu\,min\,um} + (1/hA)_{conv.}}$$

$$= \frac{(85-25)\ X\ 10^{-4}}{(0.5\ X\ 10^{-4}) + (0.002/238) + (1/1000)} = 5.667\ W$$

16. Approximately 10^6 discrete electrical components can be placed on a single integrated circuit (chip), with electrical heat dissipation as high as 30,000 W/m^2. The chip, which is very thin, is exposed to a dielectric liquid at its outer surface, with h_o = 1000 W/m^2. K and $T_{\infty,o}$ = 20 °C, and is joined to a circuit board at its inner surface. The thermal contact resistance between the chip and the board is 10^{-4} m^2.K/W. and the board thickness and thermal conductivity are L_b = 5 mm and k_b = 1 W/m.K, respectively. The other surface of the board is exposed to ambient air for which h_i = 40 W/m^2.K and $T_{\infty,i}$ = 20 °C.

(a) Sketch the equivalent thermal circuit corresponding to steady-state conditions. In variable form, label appropriate resistances, temperatures, and heat fluxes.
(b) Under steady-state conditions for which the chip heat dissipation is q_c'' = 30,000 W/m^2. What is the chip temperature?
(c) The maximum allowable heat flux $q_{c,m}''$, is determined by the constraint that the chip temperature must not exceed 85°C. Determine $q_{c,m}''$ for the foregoing conditions. If air is used in lieu of the dielectric liquid, the convection coefficient is reduced by approximately an order of magnitude. What is the value of $q_{c,m}''$ for h_o = 100 W/m^2.K? With air cooling, can significant improvements be realized by using an aluminum oxide circuit board and/or by using a conductive paste at the chip/board interface for which $R_{t,c}''$ = 10^{-5} m^2.K/W?



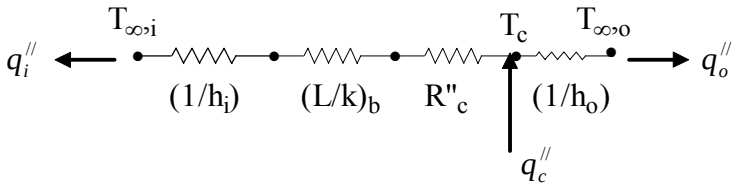
Given data: chip joined to a circuit board and its electrical heat dissipation, board properties, and coolant fluids conditions.

Assumptions:

(a) Steady-state conditions
(b) Neglect the radiation heat transfer.
(c) One-dimensional conduction.
(d) Neglect chip thermal resistance.

Solution:

(a) The equivalent thermal circuit as shown



(b) According to the thermal circuit, the chip heat dissipation is

$$q_c'' = q_i'' + q_o''$$

$$= \frac{T_c - T_{\infty,i}}{R_c'' + (L/k)_b + (1/h_i)} + \frac{T_c - T_{\infty,o}}{(1/h_o)}$$

$$30000 = \frac{T_c - 20}{(10^{-4}) + (0.005/1) + (1/40)} + \frac{T_c - 20}{(1/1000)}$$

Then the chip temperature is

$$T_c = 49\ ^{o}\text{C}$$

(c) At chip temperature 85 °C, the maximum allowable heat flux $q_{c,m}''$ is

$$q_{c,m}'' = q_i'' + q_o''$$

$$= \frac{T_c - T_{\infty,i}}{R_c'' + (L/k)_b + (1/h_i)} + \frac{T_c - T_{\infty,o}}{(1/h_o)}$$

$$q_{c,m}'' = \frac{85 - 20}{(10^{-4}) + (0.005/1) + (1/40)} + \frac{85 - 20}{(1/1000)} = 67160\ W/m^2$$

The maximum allowable heat flux $q''_{c,m}$ at h_o= 100 W/m^2.k,

$$q''_{c,m} = q''_i + q''_o$$
$$= \frac{T_c - T_{\infty,i}}{R''_c + (L/k)_b + (1/h_i)} + \frac{T_c - T_{\infty,o}}{(1/h_o)}$$
$$q''_{c,m} = \frac{85-20}{(10^{-4}) + (0.005/1) + (1/40)} + \frac{85-20}{(1/100)} = 8660\ W/m^2$$

At an aluminum oxide circuit board (k = 38 W/m.K), the maximum allowable heat flux $q''_{c,m}$ is

$$q''_{c,m} = q''_i + q''_o$$
$$= \frac{T_c - T_{\infty,i}}{R''_c + (L/k)_b + (1/h_i)} + \frac{T_c - T_{\infty,o}}{(1/h_o)}$$
$$q''_{c,m} = \frac{85-20}{(10^{-4}) + (0.005/38) + (1/40)} + \frac{85-20}{(1/100)} = 9076\ W/m^2$$

By using a conductive paste at the chip/board interface for which $R''_{t,c}$ = 10^{-5} m^2.K/W, the maximum allowable heat flux $q''_{c,m}$ is

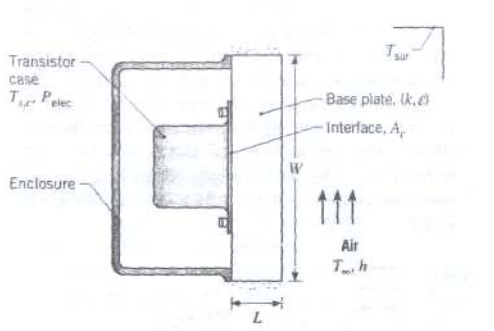
$$q''_{c,m} = q''_i + q''_o$$
$$= \frac{T_c - T_{\infty,i}}{R''_c + (L/k)_b + (1/h_i)} + \frac{T_c - T_{\infty,o}}{(1/h_o)}$$
$$q''_{c,m} = \frac{85-20}{(10^{-5}) + (0.005/1) + (1/40)} + \frac{85-20}{(1/100)} = 8666\ W/m^2$$

Using an aluminum oxide circuit board gives higher maximum allowable heat flux $q''_{c,m}$ than using conductive paste at the chip/board interface.

17. Consider a power transistor encapsulated in an aluminum case that is attached at its base to a square aluminum plate of thermal conductivity k = 240 W/m.K, thickness L = 6 mm, and width W = 20 mm. The case is joined to the plate by screws that maintain a contact pressure of 1 bar, and the back surface of the plate transfers heat by natural convection and radiation to ambient air and large surroundings at $T_\infty = T_{sur}$ = 25 °C. The surface has an emissivity of ε = 0.9, and the convection coefficient is h = 4 W/m^2.K. The case is completely enclosed such that heat transfer may be assumed to occur exclusively through the base plate.

(a) If the air-filled aluminum-to-aluminum interface is characterized by an area of A_c = 2 x 10^{-4} m^2 and a roughness of 10 μ.m. what is the maximum allowable power dissipation if the surface temperature of the case, $T_{s,c}$, is not to exceed 85 °C?

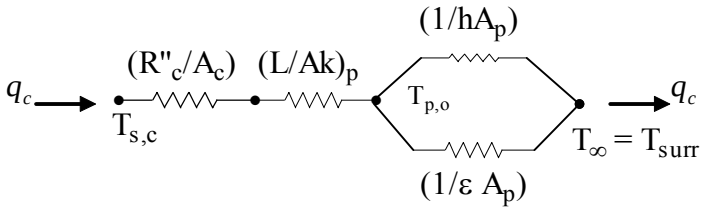
(b) The convection coefficient may be increased by subjecting the plate surface to a forced flow of air. Explore the effect of increasing the coefficient over the range $4 \leq h \leq 200$ W/ m^2.K.



Given data: A power transistor attached at its base to a square aluminum plate with a contact pressure of 1 bar, the plate whose emissivity of ε transfers heat by natural convection and radiation to ambient air and large surroundings.

Assumptions:
(a) Steady-state conditions.
(b) One-dimensional conduction.
(c) Heat transfers occur exclusively through the base plate only.

Solution:
(a) For air interfacial fluid between the aluminum case and the aluminum plate with a roughness 10μ.m, and 1 bar contact pressure. Then the contact resistance $R_c^{//} = 2.75 \times 10^{-4}$ m^2.K/W.
The thermal circuit represented as shown



According to the thermal circuit, the maximum allowable power dissipation at $T_{s,c} = 85$ °C.

$$P_{\max} = q_c = \frac{T_{s,c} - T_{p,o}}{R_c^{//} / A_c + (L/Ak)_p} = \frac{T_{p,o} - T_\infty}{(1/hA_p)} + \frac{\sigma(T_{p,o}^4 - T_{surr}^4)}{(1/\varepsilon A_p)}$$

To get the plate out side temperature $T_{p,o}$,

$$\frac{358 - T_{p,o}}{(2.75\,X\,10^{-4})/(2\,X\,10^{-4}) + (0.006/240(0.02)^2)} = \frac{T_{p,o} - 298}{1/4(0.02)^2} + \frac{5.67\,X\,10^{-8}(T_{p,o}^4 - 298^4)}{1/0.9(0.02)^2}$$

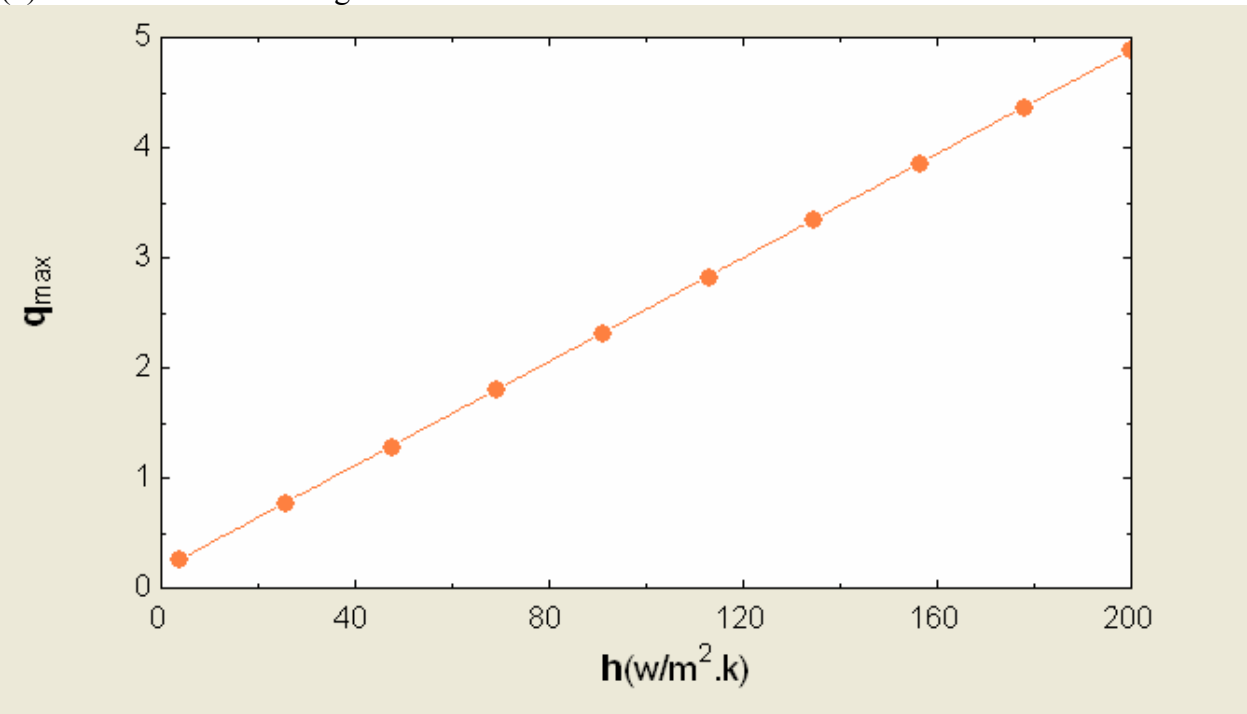
By trial and error,

$$T_{p,o}=357\ ^{o}\text{C}$$

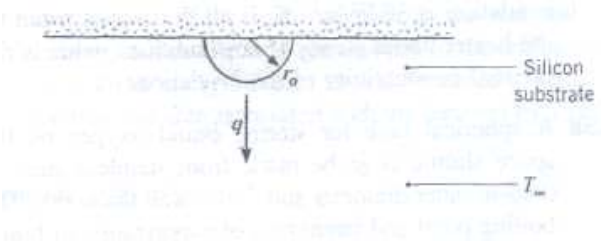
The maximum allowable power dissipation is

$$P_{\max}=q_c=\frac{T_{s,c}-T_{p,o}}{R_c''/A_c+(L/Ak)_p}=\frac{1}{1.4375}=0.5\,W$$

(b) The effect of increasing the out side convection coefficient



18. A transistor, which may be approximated as a hemispherical heat source of radius r_o = 0.1 mm, is embedded in a large silicon substrate (k = 125 W/m.K) and dissipates heat at a rate q. All boundaries of the silicon are maintained at an ambient temperature of T_∞ = 27 °C, except for a plane surface that is well insulated. Obtain a general expression for the substrate temperature distribution and evaluate the surface temperature of the heat source for q = 4 W.



Given data: A heat source embedded in a large silicon substrate, source and substrate boundary conditions.
Require: substrate temperature distribution and surface temperature of heat source for q = 4 W.
Assumption:

(a) Steady-state conditions.
(b) One-dimensional conduction.

Solution:
From energy equation reduced to

$$\frac{1}{r^2}\frac{d}{dr}(kr^2\frac{dT}{dr}) = 0$$

At constant silicon thermal conductivity

$$\frac{d}{dr}(r^2\frac{dT}{dr}) = 0$$

By integration to the substrate radius

$$r^2\frac{dT}{dr} = C_1$$

$$T(r) = -\frac{C_1}{r} + C_2$$

Boundary conditions
$T(\infty) = T_\infty$, and $T(r_o) = T_s$

Then the constants

$C_2 = T_\infty$
$C_1 = r_o(T_\infty - T_s)$

The substrate temperature distribution

$$T(r) = (T_s - T_\infty)r_o / r + T_\infty$$

The heat rate is

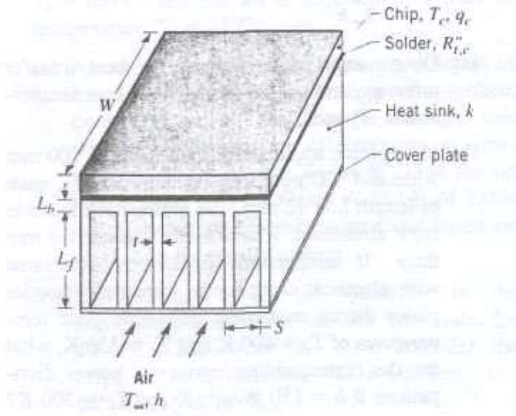
$$q = -kA\frac{dT}{dr} = -k(2\pi r^2)\left(-(T_s - T_\infty)r_o / r^2\right) = 2\pi r_o(T_s - T_\infty)$$

The surface temperature of heat source for q = 4 W is

$$T_s = 4/125(2\pi \text{ X}10^{-4}) + 27 = 78\ ^oC$$

21. An isothermal silicon chip of width W = 20 mm on a side is soldered to an aluminum heat sink (k = 180W/m.K) of equivalent width. The heat sink has a base thickness of L_b =3 mm and an array of rectangular fins, each of length L_f = 15 mm. Air flow at T_∞ = 20 °C is maintained through channels formed by the fins and a cover plate, and for a convection coefficient of h = 100 W/m^2.K, a minimum fin spacing of 1.8 mm is dictated by limitations on the flow pressure drop. The solder joint has a thermal resistance of $R''_{t,c}$ = 2 x 10$^-$6 m^2.K.

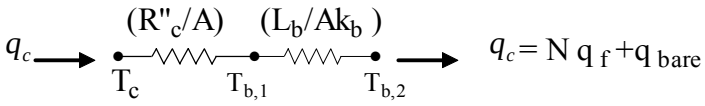
Consider limitations for which the array has N = 11 fins, in which case values of the fin thickness t = 0.182 mm and pitch S = 1.982 mm are obtained from the requirements that W= (N - 1) S + t and S - t = 1.8 mm. If the maximum allowable chip temperature is T_c = 85 °C, what is the corresponding value of the chip power q_c? An adiabatic fin tip condition may be assumed, and air flow along the outer surfaces of the heat sink may be assumed to provide a convection coefficient equivalent to that associated with air flow through the channels.



Given data: An isothermal silicon chip produces electric power, and attached to an aluminum heat sink with prescribed dimensions.
Require: (a) The maximum allowable chip power q_c at maximum chip temperature with An adiabatic fin tip condition.
Assumptions:

(a) Steady-state conditions.
(b) One-dimensional conduction.
(c) Heat transfers occur exclusively through the base of the heat sink only.
(d) An adiabatic fin tip condition.

Solution:
The thermal circuit represented as shown



From the thermal circuit, the chip power equals

$$q_c = \frac{\Delta T}{\sum R} = \frac{T_c - T_{b2}}{(R_c^{//} / A) + (L_b / Ak_b)}$$

Also the Chip power equals the summation of the fin array heat transfers and the unfinned (bare) heat transfer area,

$$q_c = N\, q_f + q_{bare} = N\, M \tanh mL_f + hA_{bare}(T_{b2} - T_\infty)$$
$$= \frac{T_c - T_{b2}}{(R_c^{//} / A) + (L_b / Ak_b)} = \frac{T_c - T_{b2}}{\Psi}$$

Where:

$M = (T_{b2} - T_\infty)\sqrt{hPk_f A_c} = (T_{b2} - T_\infty)\sqrt{2h(W+t)k_f Wt}$

A_c = Fin contact area

$m = \sqrt{\frac{hP}{k_f A_c}} = \sqrt{\frac{2h(W+t)}{k_f Wt}}$

$\Psi = (R_c^{//} / A) + (L_b / Ak_b)$

A = Cross sectional area of the base flow heat transfer

$A = [S(N-1) + t]W$

$A_{bare} = A - NtW = (s-t)(N-1)W$

The base-fin temperature T_{b2} equals

$$T_{b2} = T_c - \Psi N\, M \tanh mL_f - \Psi hA_{bare}(T_{b2} - T_\infty)$$

For prescribed conditions, the base-fin temperature,

$$T_{b2} = 83.5\ ^oC$$

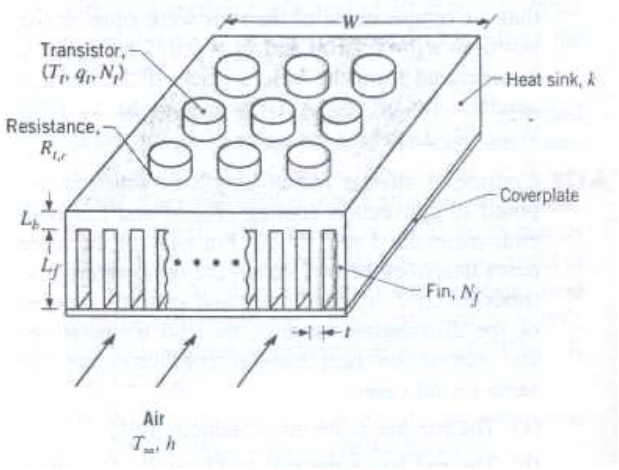
Then the maximum allowable chip power,

$$q_e = 32\ W$$

22. A 3 x 3 array of power transistors is attached to an aluminum heat sink (k = 180 W/m.K) of width W = 150 mm on a side. The thermal contact resistance between each transistor and the heat sink is $R_{t,c}$ = 0.045 K/W. The heat sink has a base thickness of L_b = 6 mm and an array of N_f = 25 rectangular fins, each of thickness t = 3 mm. Cooling is provided by air flow through channels formed by the fins and a cover plate, as well as by air flow along the two sides of the heat sink (the outer surfaces of the outermost fins).

(a) Consider conditions for which the fin length is L_f = 30 mm, the temperature of the air is T_∞ = 27 °C, and the convection coefficient is h = 100 W/m^2.K. If the maximum allowable transistor temperature is T_s = 100 °C, what is the maximum allowable power dissipation, q per transistor? An adiabatic fin tip condition may be assumed.

(b) Explore the effect of variations in the convection coefficient and fin length on the maximum allowable transistor power.



Given data: A 3x3 array of power transistors produces electric power, and attached to an aluminum heat sink with prescribed dimensions.

Require: (a) The maximum allowable power, q_t per transistor at maximum transistor temperature with an adiabatic fin tip condition, (b) effect of variations in the convection coefficient and fin length on the maximum allowable transistor power.

Assumptions:

(a) Steady-state conditions.
(b) One-dimensional conduction.
(c) Heat transfers occur exclusively through the base of the heat sink only.
(d) An adiabatic fin tip condition.
(e) All transistors at same temperatures.

Solution:

(a)The thermal circuit represented as shown

$$q_t \longrightarrow \underset{T_t}{\bullet}\!\!\sim\!\!\sim\!\!\underset{T_{b,1}}{\bullet}\!\!\sim\!\!\sim\!\!\underset{T_{b,2}}{\bullet} \longrightarrow q_t = N_f q_f + q_{bare}$$

(R_c between T_t and $T_{b,1}$; (L_b/Ak_b) between $T_{b,1}$ and $T_{b,2}$)

From the thermal circuit, the total transistors power equals

$$q_t = \frac{\Delta T}{\sum R} = \frac{T_t - T_{b2}}{R_c + (L_b / Ak_b)}$$

Also the total transistors power equals the summation of the fins heat transfers and the unfinned (bare) heat transfer area,

$$q_t = N_f\, q_f + q_{bare} = N_f\, M \tanh mL_f + hA_{bare}(T_{b2} - T_\infty)$$
$$= \frac{T_t - T_{b2}}{R_c + (L_b / Ak_b)} = \frac{T_t - T_{b2}}{\Psi}$$

Where:

$M = (T_{b2} - T_\infty)\sqrt{hPk_f A_c} = (T_{b2} - T_\infty)\sqrt{2h(W+t)k_f Wt}$

A_c = Fin contact area

$m = \sqrt{\frac{hP}{k_f A_c}} = \sqrt{\frac{2h(W+t)}{k_f Wt}}$

$\Psi = R_c + (L_b / Ak_b)$

A = Cross sectional area of the base flow heat transfer

$A = W^2$

$A_{bare} = A - N_f tW$

The base-fin temperature T_{b2} equals

$$T_{b2} = T_t - \Psi N_f M \tanh mL_f - \Psi hA_{bare}(T_{b2} - T_\infty)$$

For prescribed conditions, the base-fin temperature,

$$T_{b2} = 63.27\ ^oC$$

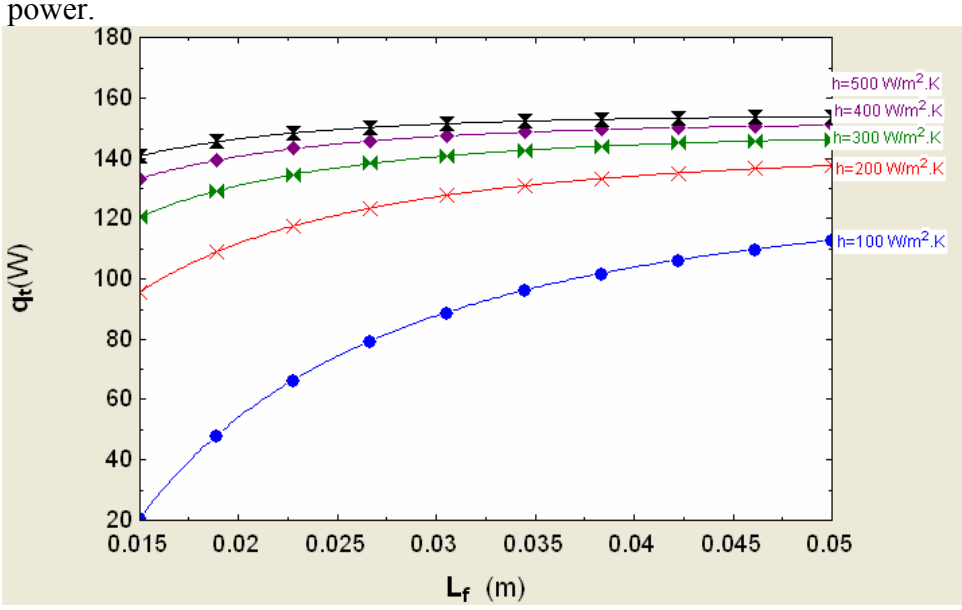
Then the maximum allowable total transistors power,

$$q_t = 790\ W$$

The maximum allowable transistors power per transistor,

$$q_t = 790/9 = 87.7\ W$$

(b) Effect of variations in the convection coefficient and fin length on the maximum allowable transistor power.



23. The interface temperature of an electronic assembly dissipating 10 W must be limited to 40 ^{o}C in a 50 ^{o}C environment. It is assumed that all of the generated heat will be removed by thermoelectrics and that heat absorbed from the environment is negligible. The interface temperature difference between the assembly and the thermoelectric can be held to 2 ^{o}C. The temperature difference between the thermoelectric and ambient can be held to 8 ^{o}C.
The bismuth telluride element used has a length of 0.3 cm and a cross-area of 0.01 cm^2.
Determine the size and performance characteristics of the thermoelectric temperature control device.
Knowing that

- The equivalent material properties of the thermoelectric couples is
  $\rho_e = 0.00267\ \Omega$.cm
  $\alpha_e = 425 \times 10^{-6}$ V/K
  $k_e = 0.00785$ W/cm.K
- Design for maximum refrigeration capacity.

Solution:
$T_h = 58\ ^{o}C = 331$ K
$T_c = 42\ ^{o}C = 315$ K
L = 0.3 cm
A = 0.01 cm^2

Overall electric resistance (R) = (ρ_e) (L/A)
$= 0.00267\ (0.3 / 0.01)$
$= 0.08\ \Omega$
Conduction coefficient (C) = (k_e) (A/L)
$= (0.00785)\ (0.01 / 0.3)$
$= 2.6 \times 10^{-4}$ W/K
Figure of merit (Z) = $\alpha_e{}^2 / RC$
$= (425 \times 10^{-6})^2 / (0.08 \times 2.6 \times 10^{-4})$
$= 8.684 \times 10^{-3}\ K^{-1}$

1- Number of couples required.
$Q_C = Q_C\ (max) = N\ C\ [(Z\ T_c^2)/2 - (T_h - T_c)]$
$10 = N\ (2.6 \times 10^{-4})\ [0.5\ (8.684 \times 10^{-3} \times (315)^2) - (16)]$
$N \approx 94$ couples

2- Rate of heat rejection to the ambient (Q_h).
$I_{opt.} = (\alpha_e)\ T_c / R$
$= (425 \times 10^{-6}) \times 315 / 0.08$
$= 1.67$ A
Then
$Q_h = N\ [(\alpha_e)\ T_h \times I_{opt} - C\ (T_h - T_c) + I^2_{opt}\ R/2]$
$= 94\ [(425 \times 10^{-6})\ 331 \times 1.67 - 2.6 \times 10^{-4}\ (16) + (1.67)^2\ 0.08 / 2]$
$= 32.2$ W

3- The COP.
$COP = Q_C / P_{in}$
P_{in} (Power input by power source to the thermoelectric) = $Q_h - Q_C$
= 32.2– 10 = 22.2 W
$COP = 10 / 22.2$
$= 0.45$

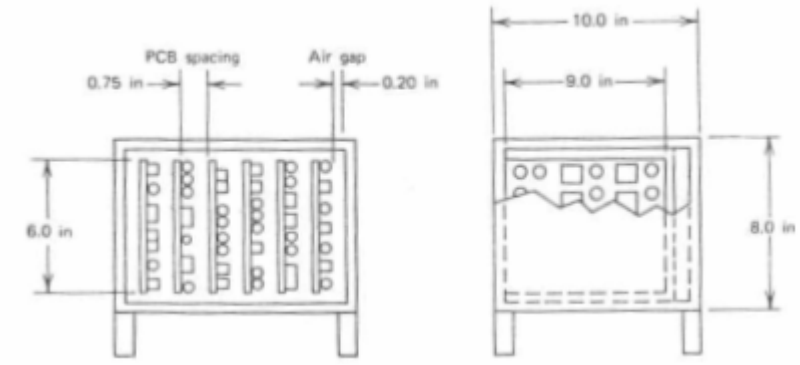
4- The voltage drop across the d.c. power source.
The voltage drop (ΔV) = P_{in} / I
= 22.2 / 1.67
= 13.3 volt

5- Size of the thermoelectric device.
The module size is approximately three times the element area. Since each couple is composed of two elements, the module area becomes

$A_{module} = 2(0.01)\ (94) \times 3 = 5.64\ cm^2$

which can be accommodated in a package measuring 2.38 cm on a side.

24. An electronic chassis was designed for natural convection cooling, so that a clearance of 0.75 in (1.905 cm) was provided between the PCBs and components. However, a design change required the addition of another PCB, which might reduce the clearance too much unless the new PCB is placed very close to the side wall of the chassis, with a clearance of only 0.20 in (0.51 cm). The PCB measures 6 x 9 in and dissipates 5.5 watts. The electronic chassis must operate at sea level conditions in a maximum ambient temperature of 43.3 °C. The maximum allowable component surface temperature is 100 °C with the chassis shown in Figure below. The aluminum chassis has a polished finish that has a low emissivity, so that the heat lost by radiation is small. The PCB construction only allows heat to be removed from the component mounting face. Determine if the design is adequate.



PCB spaced close to an end bulkhead

Solution:

Heat from the components must flow to the outside ambient. This will require the heat to flow across two major resistance areas, the internal air gap of 0.20 in (R_1) and the external convection film (R_2) with neglecting the chassis wall resistance, as shown in the following figure.

The thermal conductivity of the air in the air gap is unknown, so that an average air temperature of 80 °C is assumed and verified later. Determine the resistance with the convection coefficient for the 0.20 in air gap.

$$R_1 = \frac{1}{h_{AG} A}$$

Where:

k = 0.03 W/m.K

L = 0.20 in = 0.005 m

For small space enclosure, the air gap convection coefficient can be obtained as shown

$$h_{AG} = k / L$$

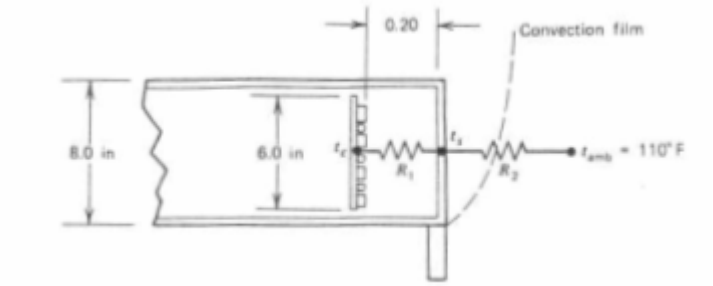
$$= 0.03 / 0.005 = 6 \text{ W/m}^2\text{.K}$$

A = 6 x 9 = 54 in^2

= 0.035 m^2

Then: $R_1 = \frac{1}{6 \text{ x } 0.035} = 4.762 \ ^{\circ}\text{C/W}$

The external convection coefficient must be estimated because the temperature rise from the surface of the chassis to the ambient is unknown.



Thermal resistances in the heat flow path from PCB components to the outside ambient

In general, natural convection coefficient for this type of structure will range from about 5 to about 10 W/m^2.K. A value of 7.5 W/m^2.K assumed to start. This can be changed if the analysis shows there is a large error.

$$R_2 = \frac{1}{h_c A}$$

Where:

h_c = 7.5 W/m^2.K

A = 8 x 10 in^2

$= 0.052\ m^2$

Then: $R_2 = \dfrac{1}{7.5 \text{ x } 0.052} = 2.58\ ^oC/W$

The temperature rise across each thermal resistor is determined as

For resistor R_1: $\Delta t_1 = QR_1 = 5.5 \text{ x } 4.762 = 26.2\ ^oC$

For resistor R_2: $\Delta t_2 = QR_2 = 5.5 \text{ x } 2.58 = 14.2\ ^oC$

The natural convection coefficient was assumed to be 7.5 $W/m^2.K$. The actual value can now be determined from Equation 7.5 using vertical chassis wall height of 8.0 in.

$$\overline{Nu} = \frac{\bar{h}L}{k} = c(\text{Gr Pr})^m$$

$$= c(Ra)^m$$

The constants c, m is given in Table 7.1 for the uniform surface temperature case. The fluid properties are evaluated at mean film temperature (T_f) where $T_f = (T_s + T_\infty)/2$.

$$\text{Gr} = \frac{g\beta(T_S - T_\infty)L^3}{\nu^2}$$

Assume $T_s = T_\infty + \Delta t_2 = 43.3 + 14.2 = 57.5\ ^oC$

$T_f = 50.4\ ^oC = 323.4\ K$

$\beta = 1/323.4\ K^{-1}$

$\nu = 18.4 \text{ x } 10^{-6}\ m^2/s$

$k = 0.02815\ W/m.K$

$Pr = 0.7035$

At $$Ra = \frac{9.81 \text{x} (1/323.4)(14.2)(0.203)^3}{(18.4 \text{x} 10^{-6})^2} \text{x } 0.7035 = 10.717 \text{x} 10^6$$

Then: c = 0.59, m= 0.25

The natural convection coefficient is 4.67 $W/m^2.K$. It nearly far from the assumed value, then by another trial with $h_c = 4.67\ W/m^2.K$.

Then: $R_2 = \dfrac{1}{4.67 \text{ x } 0.052} = 4.12\ ^oC/W$

The temperature rise across each thermal resistor is determined as

For resistor R_1: $\Delta t_1 = QR_1 = 5.5 \text{ x } 4.762 = 26.2\ ^oC$

For resistor R_2: $\Delta t_2 = QR_2 = 5.5 \text{ x } 4.12 = 22.66\ ^oC$

Assume $T_s = T_\infty + \Delta t_2 = 43.3 + 22.66 = 65.96\ ^oC$

$T_f = 54.63\ ^oC = 327.63\ K$

$\beta = 1/327.63\ K^{-1}$

$\nu = 18.67 \text{ x } 10^{-6}\ m^2/s$

$k = 0.02834\ W/m.K$

$Pr = 0.703$

At $$Ra = \frac{9.81 \text{x} (1/327.63)(22.66)(0.203)^3}{(18.67 \text{x} 10^{-6})^2} \text{x } 0.703 = 11.447 \text{x} 10^6$$

Then: c = 0.59, m= 0.25

Then the natural convection coefficient is 4.8 W/m^2.K.
This compares well with the previous assumed value.
The surface temperature of the component on the end PCB can be determined as follow:

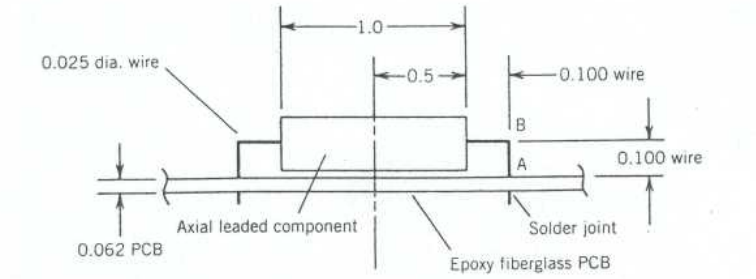
$$t_c = t_\infty + \Delta t_1 + \Delta t_2$$
$$= 43.3 + 26.2 + 22.66 = 92.16\ ^\circ\text{C}$$

The average air temperature in the gap between the wall and the component can now be determined. A temperature of 80 °C is assumed to obtain the air thermal conductivity.
The average air temperature in the gap is obtained as

$$t_{av} = \frac{t_c + t_s}{2} = \frac{92.16 + (43.3 + 22.66)}{2} = 79.06\ ^\circ\text{C}$$

This compares well with the assumed value.
Since the component surface temperature is below the maximum value of 100 °C, the design is satisfactory.
If the inside and outside surfaces of the chassis are painted any color except silver, the heat transfer by radiation will be increased and the surface of the PCB will be cooler.

25. Determine the axial force in the lead wire for the resistor shown in figure below, when bending of the PCB is included in the analysis over a temperature cycling range from -50 to +90 °C, which produce total horizontal displacement expected at the top of the wire will be 0.0003 in.
Assuming that:
E_W = 16 x 10^6 lb/in^2 (copper wire modulus elasticity)
E_P = 1.95 x 10^6 lb/in^2 (PCB modulus of elasticity)



Dimensions of axial leaded resistor throughhole mounted in a PCB (all dimensions in inches)

Solution:
The axial load in the lead wire induced by the different TCE will produce an overturning moment in the PCB and force it to bend. Considering the pivot point to be at the lead wire solder joint, the angular rotation of the lead wire (for small angles) must be the same as the angular rotation of the PCB. The PCB angular rotation will be

$$\theta = \frac{ML_P}{2E_P I_P}$$

Then combined deflection of the bending wire and the rotating PCB is

$$X = \frac{PL_W^3}{7.5E_W I_W} + \frac{RML_P}{2E_P I_P}$$

Reference subscripts W and P are added for the wire and PCB respectively.

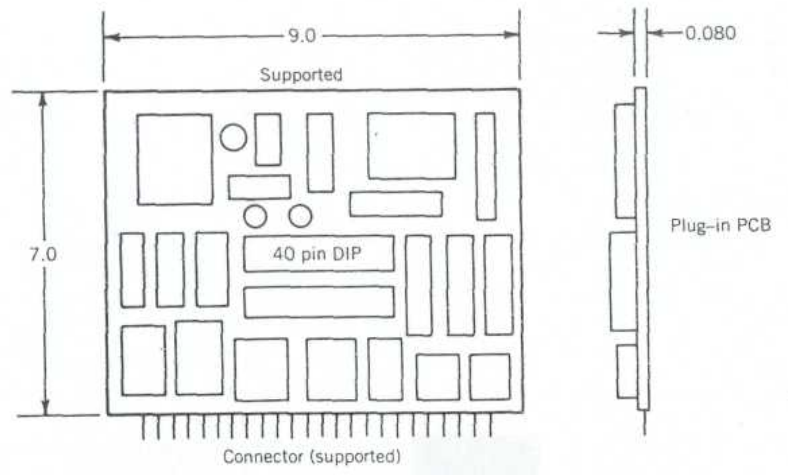
Where:
X = 0.0003 in
E_W = 16 x 10^6 Ib/in^2 (copper wire modulus elasticity)
$I_W = \pi (d^4)/4 = 1.917 \times 10^{-8}$ in^4
d = 0.025 in
R = height of wire plus one wire diameter into the PCB for wire in bending
= 0.1 + 0.025 = 0.125 in (moment arm length)
L_W = effective wire length = length of wire plus one wire diameter
= 0.1 +0.025 = 0.125 in
E_P = 1.95 x 10^6 Ib/in^2 (PCB modulus of elasticity)
L_P = length of PCB between component lead wires
= 1 + 2(0.1) = 1.2 in (PCB length)
h = 0.062 in (PCB thickness)
b = effective width of PCB for bending = 30 x h = (30) (0.062) = 1.86 in (effective width of PCB assuming no other similar components on PCB)
$I_P = bh^3/12 = (1.86)(0.062)^3/12 = 3.694 \times 10^{-5}$ in^4
M = RP = 0.125 P (bending moment on PCB)

Substitute to get the wire load when PCB bends:

$$0.0003 = \frac{P(0.125)^3}{7.5(16\times10^6)(1.917\times10^{-8})} + \frac{(0.125)(0.125P)(1.2)}{2(1.95\times10^6)(3.69\times10^{-5})}$$

$$P = 0.3066 \text{ Ib}$$

26. Determine the resonant frequency of a rectangular plug-in epoxy fiberglass PCB simply supported (or hinged) on all four sides, 0.080 in thick, with a total weight of 1.0 pounds, as shown in figure. (Note: All dimensions in inches)
Assuming that:
E = 2 x 10^6 Ib/in^2 (PCB modulus of elasticity)
μ = 0.12 (Poisson's ratio, dimensionless)



Solution:

The following information is required for a solution:

E = 2 x 10^6 Ib/in^2 (epoxy fiberglass modulus of elasticity)

h = 0.080 in (PCB thickness)

μ = 0.12 (Poisson's ratio, dimensionless)

W = 1.0 Ib (weight)

a = 9.0 in (PCB length)

b = 7.0 in (PCB width)

g = 386 in/sec^2 (acceleration of gravity)

$$D = \frac{(2 \text{ x } 10^6)(0.08)^3 h^3}{12(1-(0.12)^2)} = 86.6 \quad \text{Ib in} \quad \text{(stiffness)}$$

$$\rho = \frac{1.0}{(386)(9)(7)} = 0.431 \text{ x} 10^{-4} \quad \frac{\text{Ibsec}^2}{\text{in}^3}$$

Then the resonant frequency of PCB is

$$f_n = \frac{\pi}{2}\sqrt{\frac{86.6}{0.431 \text{ x } 10^{-4}}\left(\frac{1}{(9)^2}+\frac{1}{(7)^2}\right)}$$

$$= 72.9 \text{ HZ}$$